Application Brief

Design Smaller Safe Torque Off (STO) Systems Using Integrated 3-Phase Smart Gate Drivers

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The evolution of industrial applications involving motorization and electrification provides benefits such as intelligent automation, and advanced productivity. Conventional manual work is being replaced with the assistance and interaction of automated equipment. This evolution results in humans getting more exposed to hazards from both machines and actuators; a cause of concern during operation. To reduce the risks of the hazards, there are many functional safety standards which help provide guidance for designing safety systems.

One of the functional safety standards, IEC 61800-5-2, defines a safety function called Safe Torque Off (STO). To quote from IEC 61800-5-2, STO is defined as the function *to prevent force-producing power from being provided to the motor*, and is often the most basic and critical requirement if the system has a requirement to stop the motor safely and to prevent an unexpected start-up. In many cases, this STO function is designed with a size constraint of the motor system hardware. This article discusses the requirements of STO, the market trend, existing solutions, and the approach of the small STO design using DRV8350F and DRV8353F.

Market Trend and Designing Smaller Motor Systems

To implement motor drive systems including the STO function, designers often use discrete single-channel gate drivers or half-bridge gate drivers especially for AC input power stages with IGBTs. DC-fed power stages with typical supply voltages of 48-V to 60-V have strong constraints of the system hardware size, such as linear-motor transport systems, industrial collaborative robots, industrial mobile robots, or autonomous guided vehicles (AGV). These applications are looking for further reduction of system size and component count in the system.

Compared to conventional discrete gate drivers, integrated 3-phase gate drivers can help reduce system component count and system size. Texas Instruments (TI) is offering highly integrated 3-phase gate drivers with smart gate drive technology which contain configurable parameters and protection features. Visit the TI smart gate drive web site (a white paper and a video) to learn more about the architecture and the benefits of smart gate drive technology. A comparison of a discrete gate driver and an integrated gate driver is discussed in the TI blog series *A basic brush-less gate driver design Part 1, Part 2, and Part 3*. Besides these benefits, system designers need to fully understand the STO requirement and challenge of an integrated 3-phase gate driver in order to design the STO function using a 3-phase smart gate driver.

What is STO

Figure 1 shows an example of an STO implementation referring to IEC61800-5-2 Annex B. The Digital Processing Unit (MCU, processor, and so on) generates PWM pulse signals for the motor control. The gate drivers in the 3-phase power stage control the gates of the power switches (IGBT, MOSFET, and so on), and the motor rotational torque is generated. STO-A and STO-B are command signals from external devices, such as emergency stop signals and safety logic.

STO-A and STO-B commands can also be signaled from other safe stop functions like Safe Stop1 (SS1) or Safe Stop2 (SS2) which are defined in IEC61800-5-2 and stop the motor drive system in a controlled manner using motor position or current sensing information. When a STO-A (or STO-B) command is received from the external devices, the pulse inhibition channel PI-A (or PI-B) is activated to disconnect the power supply $P_{GateDriver}$ from the gate drivers. Since the power-supply voltage of the gate drivers is not available, the power switches are turned off and the motor rotation torque cannot be generated. This process results in the desired safe state of the STO function.

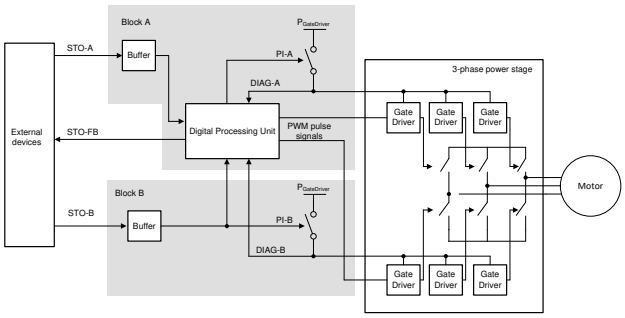

Figure 1. STO Implementation Example

- $P_{GateDriver}$: Gate-driver power supply
- PI-A(B): Pulse inhibition channel A(B)
- DIAG-A(B): Diagnosis signal channel A(B)

STO Requirements

There are two key considerations when designing the STO function: the architecture to mitigate the risk of failure, and evaluation of random faults.

1) Architecture to Mitigate the Risk of Failure

The machinery safety standard ISO 13849-1 introduces a *Category (Cat)* to describe the classification of a safety-related system architecture for the resistance to faults and its subsequent behavior. For example, Cat 3 and Cat 4 (Cat 3/4) systems require continued performance of the safety function in the presence of a single fault. The system in Figure 1 consists of two STO channels, STO-A and STO-B. If a fault exists in the STO-A channel, the motor stop function is not available through the STO-A channel anymore. If the STO-B channel is designed properly, STO-B is functional and the system can stop the motor rotation torque. In this example, the entire system can achieve the STO function in the presence of a single fault.

This architecture requirement is also discussed in another functional safety standard IEC 61508 using a different terminology, *Hardware Fault Tolerance* (HFT). A system with HFT = 1 needs to maintain the safety function in case of a single fault. Due to the redundant design of STO-A and STO-B, the system diagram in Figure 1 is considered to meet HFT = 1 and Cat 3/4 from an architecture point of view.

2) Evaluating Random Fault and Diagnosis

The IEC 61508 standard defines a quantitative target to evaluate the performance of safety function using *Safety Integrity Levels* (SIL). SIL 1 is the lowest, and SIL 3 is typically the highest requirement seen in industrial motor drive systems. One aspect of SIL is to evaluate the probability of dangerous random faults of the system. The diagnostic function of the system is also evaluated using *Performance Level* (PL) as defined in ISO 13849. The PL level uses alphabet a, b, c, d, and e to represent the reliability of the system (a is the lowest and e is the highest). For example, PLe is considered to be an equivalent level to SIL 3. In Figure 1, DIAG-A (or DIAG-B) is testing the PI-A (PI-B) function to check if the power supply can be disconnected from the gate driver as expected. In the example of IEC 61800-5-2 Annex B, the Digital Processing Unit collects the information of DIAG-A and DIAG-B, and the complied diagnostic test results of the STO-A and STO-B functions are reported to the external devices through the STO-FB feedback signal. The effectiveness of the diagnostic functions are evaluated in accordance with the requirements defined by the SIL and PL levels. Today's motor drive systems often implement the STO-A and STO-B diagnostic functions with simple discrete circuitry.

STO Design Challenges and TI Integrated 3-phase Smart Gate Drivers

If you look at the 3-phase power stage block in Figure 1, the gates of the power transistor switches are individually driven by six gate driver devices. This discrete gate driver solution is often used for the implementation of STO in the market. When designing the STO function with discrete devices, the failure modes of the power drive stage can be easily analyzed because of the simplicity of the gate driver IC.

As discussed earlier, implementing the power stage with TI integrated 3-phase smart gate drivers could be a desired solution for size constrained applications. However, when considering an integrated 3-phase smart gate driver, you might have many questions before you start designing the STO function;

- What are the detailed failure modes inside of a highly integrated 3-phase smart gate driver?
- How to connect the STO-A and STO-B channels to an integrated 3-phase smart gate driver?
- What documents for the gate driver are available from TI to help with the STO system design?
- Did TI work with a third party to validate the STO concept using a 3-phase smart gate driver?

TI recommends the new 3-phase smart gate driver family DRV8350F and DRV8353F to help you answer the questions above. DRV8350F and DRV8353F are released as Functional Safety Quality-Managed devices. Documentation is available to assist the system developer with the design of the STO function. TI has also collaborated with TUEV-SUD on the proposed system concept of the STO function using DRV8350F. The concept was evaluated in accordance with SIL 3, Cat 4 / PLe requirements. An according concept report is available from TI. The

DRV835xF device family helps to reduce system size with highly integrated smart gate drive functions, and helps the design of the STO function with Functional Safety Quality-Managed technical documentation and a concept report.

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