Application Note

Example of LED Display Screen Design Requirements Based on TLC6983

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ABSTRACT

The hardware and software design of LED display screen systems requires engineers to understand design requirements of the LED display screen and to make sure the driver performance can satisfy these requirements. There are many LED display design parameters that can confuse designers when configuring the LED driver.

This application note presents an emerging LED display end equipment example, an LED cinema screen, to help designers better understand and design the LED display screen system. The LED cinema screen example has a 1920-Hz to 7680-Hz refresh rate, 60/120-Hz frame rate, and 14-bits to 16-bits PWM resolution. This application note shows how to calculate configuration parameters step-by-step based on TI's latest Common Cathode Matrix LED Display Driver, the TLC6983.

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1 Introduction

Table 1-1 shows the typical, basic design parameters table for an LED cinema screen from the perspective of a product manager. Based on the key information of LED panel module resolution, frame rate, color depth, and refresh rate, the system engineer needs to design some basic parameters related to the LED driver that are discussed more in detail throughout this document.

Table 1-1. LED Display Screen Basic Design Parameters

Type	Parameter	Value
Physical Parameter	LED Screen Resolution	4K (3840 × 2160)
	LED Screen Pitch (mm)	2.5
	LED Box Module Resolution (dots)	384 × 216
	LED Box Module Size (Width×Hight)/(mm)	960 × 540
	LED Panel Module Resolution (dots)	96 × 108
	LED Panel Module Size (Width×Hight)/(mm)	240 × 270
Optical Parameter	Frame Rate (Hz)	60/120
	PWM Resolution/Grayscale Intensity/Color depth (bits)	14 to 16
	Refresh Rate (Hz)	1920 to 7680
	Typ./Max Brightness (nit)	48/300 (Max 500 nit at HDR cinema mode)
	Minimum Brightness (nit)	0.03
	Black level	0.005 nit or match the black level of the DCI projector
	Contrast Ratio (In darkroom)	∞ : 1
	Color Temperature (K)	6000
	Color gamut	DCI-P3
	White Point	D63 (Xw 0.3140, Yw 0.3510)
	Gamma coefficient	2.6

Figure 1-1 shows a typical 4K resolution (3840 × 2160) LED Display screen and the corresponding breakdown drawing. Within the LED panel module (96 × 108), the LED panel module is further decomposed into 18 sub-blocks (6 groups with each group having 3 sub-blocks) with each block having 32 RGB channels and 18 scans (32 × 18). The TLC6983 48x16 Common Cathode Matrix LED Display Driver with Ultra Low Power data sheet specifies that the TLC6983 can use dual devices in stackable mode to supports 32 × 32 RGB pixels (32 RGB channels and 32 scans). Why does the system engineer only uses 18 scans? What are the design considerations to consider? These questions are discussed in depth throughout this application note.

Figure 1-1. A Typical 4K LED Display With the Breakdown Drawing

2 Design Recipe

Although there are many design parameters, each design parameter is not wholly independent and has some correlation or overlap. Iterating on a design can be unavoidable to achieve the best design. The design recipe provided in this application note can be roughly divided into three parts, as described in the following sections.

2.1 Check Sub-period Number and Segment Length

The relational expressions between sub-period (or sub-frame) number, N_{sub_period}, within one frame, segment length (GCLK number per segment, line switch time excluded), N_{GCLK_seg}, refresh rate, $f_{refresh\_rate}$, frame rate, $f_{refresh\_rate}$, and PWM resolution, K, is shown in the following equations.

$$N_{sub\_period} = \frac{f_{refresh\_rate}}{f_{frame\_rate}} \quad (1)$$

$$N_{GCLK_{seg}} = \frac{2^K}{N_{sub\_period}} \quad (2)$$

For the TLC6983, the N_{sub_period} can be set as 16, 32, 48, 64, 80, 96, 112, 128, or 256 (a sub-period of 256 requires that SUBP_MAX_256 is enabled). The N_{GCLK_seg} can be 128 to 1024 GCLKs. Make sure that the sub-period number and segment length are not out of range. If these parameters are out of range, an iteration on the design or correction needs to be made.

Table 2-1 lists the calculated results for a scenario where an engineer is designing an LED panel module (at the best performance of 7680 Hz, 120 Hz). The table shows that the calculated results are within the range.

Table 2-1. Sub-period Number and Segment Length Check

Boundary Condition Check		
Maximum Sub-period number within one frame	N_{sub_period}	64
GCLK number per segment (Line switch time excluded)	N_{GCLK_seg}	1024

However, if the product manager wants the design to have a maximum refresh rate of 7680 Hz for a 24 FPS movie application, the desired output can not be achieved since the N_{sub_period} value is out of range (7680 / 24 = 320 > 256). The refresh rate needs to be lower to satisfy the boundary condition. As another example, an application with a 3840-Hz refresh rate, a 120-Hz frame rate, and a 16-bit PWM resolution can not be achieved, because N_{GCLK_seg} is out of range (t) = 2048 > 1024). The refresh rate needs to be higher or the PWM resolution needs to be lower to satisfy the boundary condition. Reducing PWM resolution is not an acceptable outcome but having a higher refresh rate does no harm to the performance of the LED display screen.

2.2 Design Scan Line Number

Figure 2-1 shows the DS-PWM algorithm with 32 lines integrated into the TLC6983.The relational expression between frame rate (f_{frame_rate}), segment length (N_{GCLK_seg}), GCLK frequency (f_{GCLK}), line switch time (T_{SW}), scan line number (N_{scan_line}), sub-period (or says sub-frame) number (N_{sub_period}), and the blank time (T_{blank}) in one frame is as following.

$$\frac{1}{f_{frame\_rate}} = \left(\frac{N_{GCLK\_seg}}{f_{GCLK}} + T_{SW}\right) \times N_{scan\_line} \times N_{sub\_period} + T_{blank} \quad (3)$$

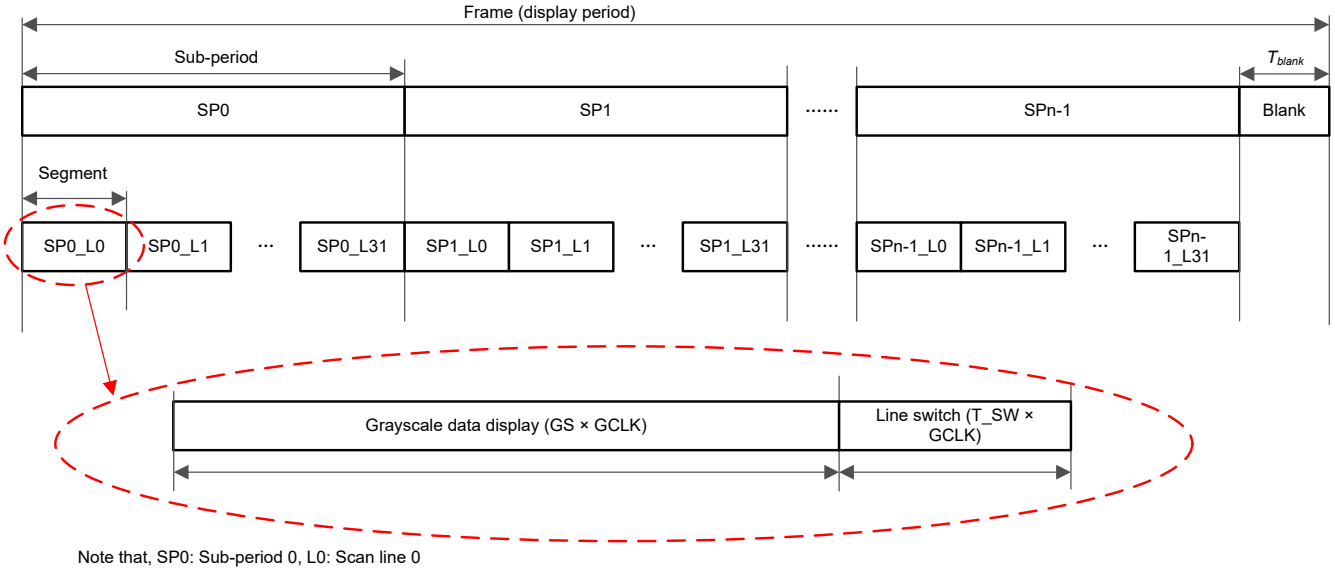

Figure 2-1. DS-PWM Algorithm With 32 Scan Lines

The maximum GCLK frequency (f_{GCLK}) allowed is 160 MHz. The minimum allowed line switch time T_{SW} can be set to 45 GCLK. However, at least 1μs to 1.5μs line switch time is recommended. The blank time (T_{blank}) is equal to 0 in ideal configurations. So, the maximum scan line number allowed is:

$$N_{max\_scan\_line} = ROUNDDOWN\left(\frac{1}{f_{frame\_rate} \times \left(\frac{N_{GCLK\_seg}}{160\ MHz} + \frac{45}{160\ MHz}\right) \times N_{sub\_period}}, 0\right) \quad (4)$$

Using Equation 4, the calculated result is 19, which is much less than the 32 scans discussed in Section 1 that can be supported by the dual TLC6983 in stackable mode. This result implies that the actual maximum available scan line number is limited to the maximum PWM resolution required by the product and the maximum GCLK frequency generated by the driver itself. Restated, achieing a very high PWM resolution and high scan line number at the same time is very difficult with a limited GCLK frequency. There is a tradeoff between the PWM resolution and scan line number. The higher the integration density (with high scan line number), the lower the PWM resolution. For instance, consider the effect of reducing resolution from 16 bits to 15 bits. The PWM resolution cannot be lowered because display effect is then lowered, instead, scan line number must be reduced. This tradeoff is one of the reasons why a products on the market can have a driver that can support 16 or higher bits but the “real” 16-bit PWM resolution is much lower. This relationship is also why some high-end products on the market have very small scan line numbers, to acquire excellent display effects (from 16-bits, 20-bits or higher PWM resolution).

Returning back to the design requirements, the LED panel module (96 × 108) has 96 columns; dual TLC6983 in stackable mode (sub-block) can support 32 × 32 RGB pixels (32 RGB channels and 32 scans). So, all RGB channels can be fully utilized (96 / 32 = 3 sub-blocks in row). A cascade device number ($N_{cascade}$) of 6 is recommended for this use case (96 / 16 = 6). The cascade number can be set higher, such as 12 devices in cascade, but more cascade devices need higher SCLK frequency (SCLK design is discussed in later sections) which can cause worse EMI, and also places more requirements on the FPGA of the controller.

For scan lines, the following relationship is considered: ROUNDUP(108 / 19, 0) = 6, 108 / 6 = 18. This calculation results in 6 sub-blocks in column. 108 is divisible by 18 and the scan line number (N_{scan_line}) can be set to 18. If the numerator is not divisible,then spacing out the scan lines as far as possible for loading sharing purpose is recommended. For example, if the maximum allowed scan line number is 16, that scan line suggests that 3 sub-blocks have 16 scan lines and 4 sub-blocks have 15 scan lines in a column.

The equation for the minimum GCLK frequency is:

$$f_{min\_GCLK} = \left(N_{GCLK\_seg} + 45\right) \times N_{scan\_line} \times N_{sub\_period} \times f_{frame\_rate} \quad (5)$$

Using the preceding figures, the result of the calculation with this equation 147.8 MHz.

Figure 2-2 shows more details of the LED panel (96x108) highlighted in Figure 1-1. The LED panel module is decomposed into eighteen 32 × 18 sub-blocks (6 groups in row). Each sub-block has the dual TLC6983 in stackable mode connection. Figure 2-3 and Figure 2-4 show the physical prototype board.

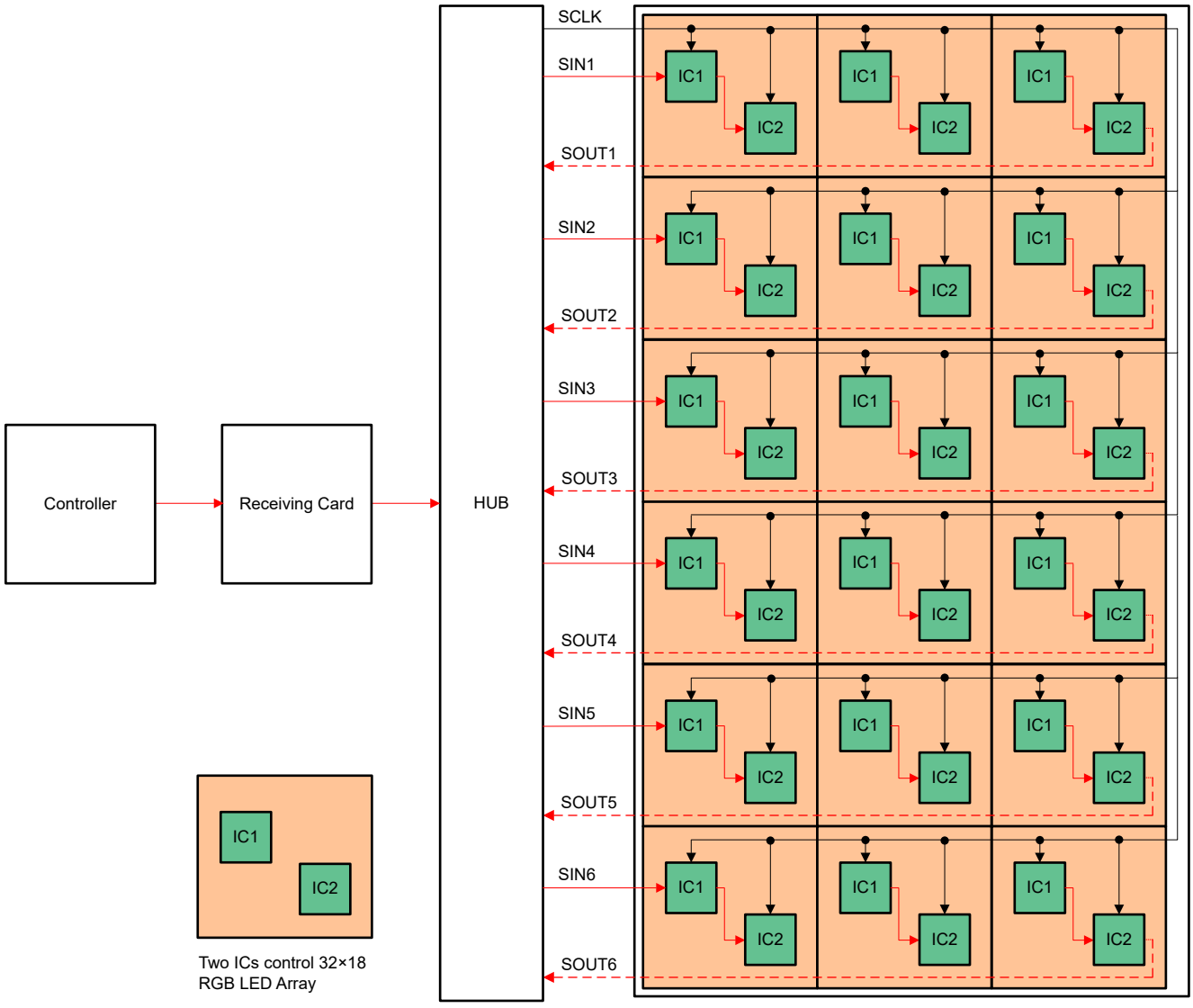

Figure 2-2. Details of the LED Panel Module (96 × 108)

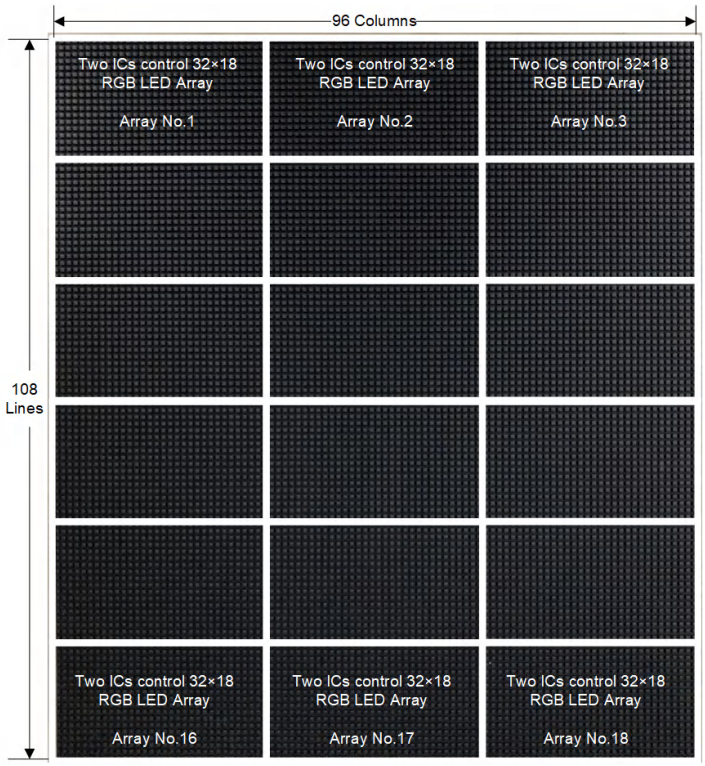

Figure 2-3. The Front of the LED Panel Module Prototype Board (96 × 108)

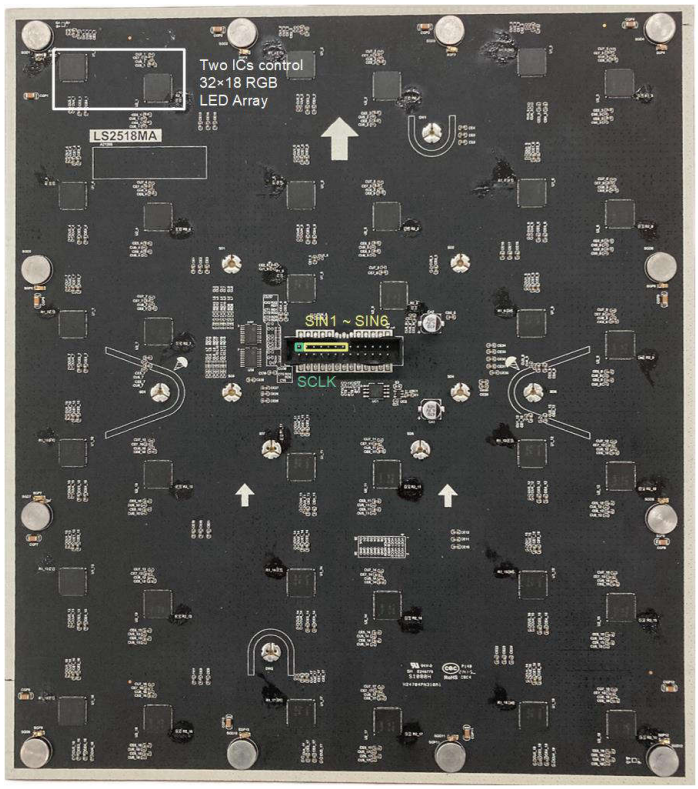

Figure 2-4. The Back of the LED Panel Module Prototype Board (96 × 108)

2.3 Design SCLK Frequency

As shown in Figure 2-1, cascaded devices compose one data stream (SIN1, SIN2…,SINx). The SCLK frequency is determined by the data volume of the data stream in each frame and frame rate. Each scan line of TLC6983 has 48-bit-wide memory for every corresponding RGB channel. If dual devices are in stackable mode (N_{stack} = 2), there are 32 channels for each sub-block. If three devices are in stackable mode (N_{stack} = 3), there are 48 channels for each sub-block.

Note that if there are unused channels in the sub-block, the FPGA controller still needs to send zero gray scale data (GS data) to the unused channels since the GS data needs to be continuously stored into the SRAM for all 16 RGB channels in each scan line. The channel counter resets to 0 after 16 gray scale data-write operations. However, there is no need to send the zero data to unused scan lines since all scan lines have been updated with new gray scale data once the line counter exceeds the scan line number.

The equation of the data volume is,

$$V_{Data} = \left(N_{scan\_line} \times (16 \times N_{mode}) \times 48 \text{ bits}\right) \times \left(\frac{N_{cascade}}{N_{mode}}\right) = \left(N_{scan\_line} \times 16 \times 48 \text{ bits}\right) \times N_{cascade} \quad (6)$$

In this example, the data volume V_{Data} = 18 × 16 × 48 × 6 = 82.944Kb.

For the data transmission, with the exception of the effective gray scale data, there is other data. Some of the other data is head bytes, a check bit, end bits, and more. The data transmission efficiency is supposed to be 80% based on empirical value.

Hence, the equation of the minimum SCLK frequency with single-edge transmission is,

$$f_{SCLK} = \frac{\left(V_{Data} \times f_{frame\_rate}\right)}{0.8} \quad (7)$$

In this example, the minimum SCLK frequency is 12.4 MHz with single-edge transmission and 6.2 MHz with dual-edge transmission. Finally, single-edge transmission of 12.5-MHz SCLK can be selected, which is generally used in an FPGA.

Table 2-2 lists the updated design requirements based on above calculations. Then engineers can start the configuration work for the driver registers to match those requirements.

Table 2-2. LED Display Screen Design Requirements Summary

Parameters	Symbol	60-Hz FPS	120-Hz FPS
Frame Rate (Hz)	f_{frame_rate}	60	120
PWM Resolution, Gray scale Intensity, or Color depth (bits)	K	16	16
Maximum Refresh Rate (Hz)	$f_{refresh\_rate}$	7680	7680
Maximum Sub-period Number within one frame	N_{sub_period}	128	64
GCLK number per segment (Line switch time excluded)	N_{GCLK_seg}	512	1024
Cascaded devices number (#)	$N_{cascade}$	6	6
Scan Lines number (#)	N_{mode}	18	18
Independent or Stackable mode device number (#)	f_{SCLK}	2	2
SCLK Frequency (MHz)	f_{min_GCLK}	12.5	12.5
Minimum GCLK frequency (MHz)	-	77	147.8
Gamma Coefficient	-	2.6	2.6
Typical Brightness (nit)	-	48	48
Color Temperature (K)	-	6000	6000

3 Summary

This application note discusses basic design parameters of LED display screen and provides a step-by-step calculation example of parameters configuration based on TI's latest Common Cathode Matrix LED Display

Driver, the TLC6983. This application note is a good reference to help engineers and new users better understand and design the LED display screen system at the onset of the application design.

4 References

- Texas Instruments, *TLC6984 48 x 16 Common Cathode Matrix LED Display Driver Evaluation Module* user's guide.
- Texas Instruments, *TLC6983 48 x 16 Common Cathode Matrix LED Display Driver Evaluation Module* EVM user's guide.

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