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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

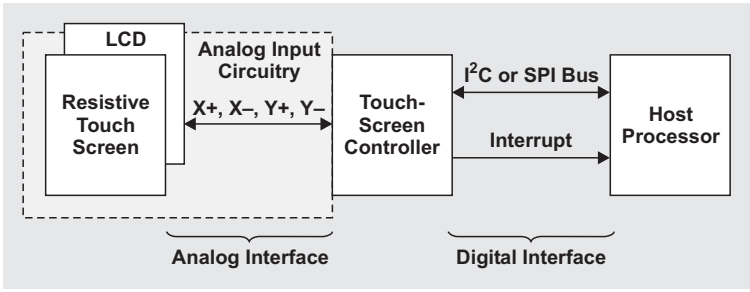
Calibration in touch-screen systems

By Wendy Fang, *Precision Analog Applications, High-Performance Analog,*
and Tony Chang, *Precision Analog Nyquist, High-Performance Analog*

Introduction

Today, more and more different fields are adopting touch screens or touch panels for applications with human/machinery or human/computer interfaces. Figure 1 is a block diagram of a touch-screen system where the touch screen sensor lies on top of the system's display, in this case an LCD panel.

Figure 1. Typical four-wire resistive touch-screen system



The touch-screen controller in Figure 1 does not need any calibration by itself. However, products or instrumentation equipped with a touch screen normally require a calibration routine upon power up because it is difficult to perfectly align a touch screen's coordinates with those of the display underneath it. Calibration is necessary when the coordinates of the area touched on the screen are not sufficiently close to the coordinates on the display. Without proper calibration, software may not respond correctly when a soft button or icon is pressed.

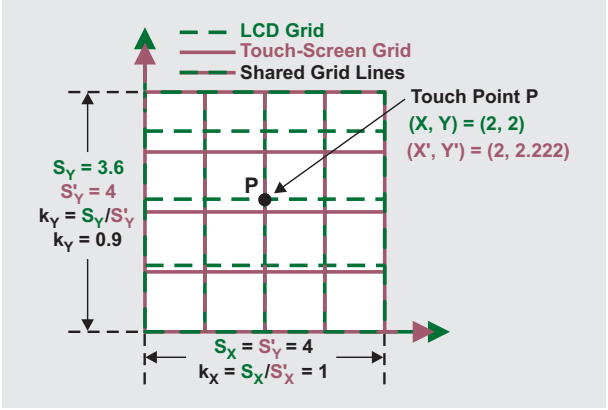
This article presents concepts and methods for the calibration of touch-screen systems. Software-programming algorithms and their implementation are also discussed.

Touch-coordinate errors

When pressure is applied to the touch screen, the touch-screen controller senses it and takes a measurement of the X and Y coordinates. Several sources of error can affect the accuracy and reliability of this measurement. The majority of these errors can be attributed to electrical noise, scaling factors, and mechanical misalignments.

Electrical noise comes from the display and backlight, the human interface, the panel surface's vibration, and the electrostatic discharge and electromagnetic pulses caused by users and their environments. This article does not address noise issues. For more information on handling noise, please see Reference 1.

Figure 2. Scaling factors on the Y axes of LCD and touch screen



Scaling factors and mechanical misalignments originate in the parts and assembly of the touch screen and the display. Typically, the touch-screen controller and display in a system do not have the same resolution, so scaling factors are needed to match their coordinates to each other. For example, consider a touch-screen system that uses an LCD with a resolution of 1024 (X coordinate) × 768 (Y coordinate) and the Texas Instruments TSC2005 touch-screen controller with 12-bit (4096 × 4096) resolution. The scaling factors to match them are $k_X = S_X/S'_X = 1024/4096 = 0.25$ for the X-axis coordinate and $k_Y = S_Y/S'_Y = 768/4096 = 0.1875$ for the Y-axis coordinate, where S_X is the LCD's X-axis resolution, S'_X is the touch-screen controller's X-axis resolution, S_Y is the LCD's Y-axis resolution, and S'_Y is the touch-screen controller's Y-axis resolution. Thus, a touch-screen controller's X coordinate, X′, should be understood by the LCD (the host) as $X = k_X \times X'$; and a touch-screen controller's Y coordinate, Y′, should be understood by the LCD (the host) as $Y = k_Y \times Y'$.

In the preceding example, k_X and k_Y are simple linear scaling factors based on the resolution specifications for the display and touch-screen controller. "Real-world" scaling factors may vary from part to part and may need to be calibrated to reduce or eliminate any mismatch. An example is shown in Figure 2, where the X-axis scale is the same on the LCD and the touch screen, or $k_X = S_X/S'_X = 1$; but the Y-axis scale on the LCD is larger than that on the touch screen, with the scaling factor of $k_Y = S_Y/S'_Y = 3.6/4 = 0.9$. Thus, a point P (X′, Y′) = (2, 2.222) on the touch screen should be scaled to (X, Y) = (2, 2) for the LCD (the host).

Mechanical misalignment between the display and the touch screen includes moving and rotation errors, as shown in Figure 3. Figure 3a shows the relative position shifts of ΔX in the X direction and ΔY in the Y direction; and Figure 3b shows the relative rotation, Δθ, between the LCD and the touch screen.

Consider a point P, read as (X′, Y′) on the touch screen. The display should read a moving error like that shown in Figure 3a as (X′ + ΔX, Y′ + ΔY). For a rotation error like that shown in Figure 3b, the point on the touch screen is (R × cosθ, R × sinθ), or on the display is [R × cos(θ–Δθ), R × sin(θ–Δθ)], where R is the distance from origin C, or (0, 0), to the point P.

Mathematical expression

Calibration of the touch screen translates the coordinates reported by the touch-screen controller into coordinates that accurately represent the point and image location on the display or LCD. The result of calibration is a set of scaling factors that allow correction of the moving and rotation errors that are due to mechanical misalignments.

Consider the point P, represented as (X, Y) on the display and (X′, Y′) on the touch panel. Counting in the scaling factor in Figure 2 and the moving and rotation errors in Figure 3, the touch-screen coordinate X can be expressed as

$$\begin{aligned} X &= k_X \times R \times \cos(\theta - \Delta\theta) + \Delta X \\ &= k_X \times R \times \cos\theta \times \cos(\Delta\theta) + k_X \times R \times \sin\theta \times \sin(\Delta\theta) + \Delta X \\ &= k_X \times X' \times \cos(\Delta\theta) + k_X \times Y' \times \sin(\Delta\theta) + \Delta X \\ &= \alpha_X \times X' + \beta_X \times Y' + \Delta X, \end{aligned} \quad \textbf{(1)}$$

where $X' = R \times \cos\theta$, $Y' = R \times \sin\theta$, $\alpha_X = k_X \times \cos(\Delta\theta)$, and $\beta_X = k_X \times \sin(\Delta\theta)$. Similarly, the touch-screen coordinate Y can be expressed as

$$\begin{aligned} Y &= k_Y \times R \times \sin(\theta - \Delta\theta) + \Delta Y \\ &= k_Y \times R \times \sin\theta \times \cos(\Delta\theta) - k_Y \times R \times \cos\theta \times \sin(\Delta\theta) + \Delta Y \\ &= k_Y \times Y' \times \cos(\Delta\theta) - k_Y \times X' \times \sin(\Delta\theta) + \Delta Y \\ &= \alpha_Y \times X' + \beta_Y \times Y' + \Delta Y, \end{aligned} \quad \textbf{(2)}$$

where $\alpha_Y = -k_Y \times \sin(\Delta\theta)$, and $\beta_Y = k_Y \times \cos(\Delta\theta)$.

From Equations 1 and 2 it is obvious that, to get the coefficients α_X, α_Y, β_X, β_Y, ΔX, and ΔY, at least three independent points are needed. The points are independent if they are not on one linear line (see Figure 4). Assuming that (X_1, Y_1), (X_2, Y_2), and (X_3, Y_3) are three independent

Figure 3. Mechanical misalignments

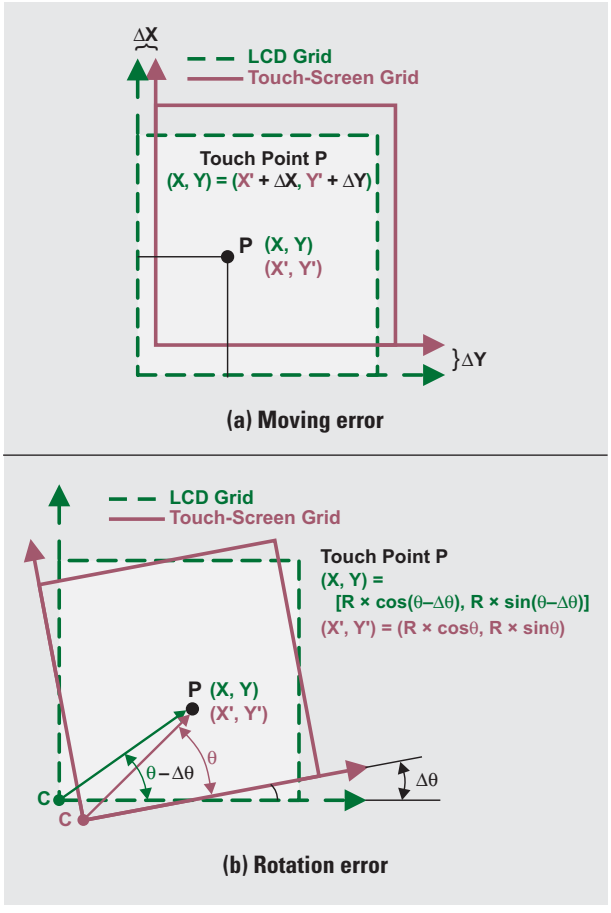
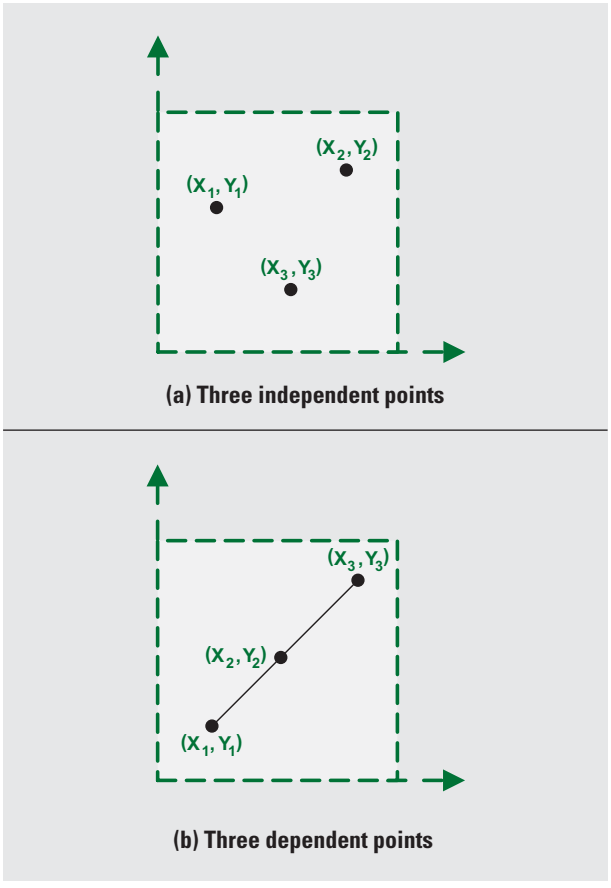


Figure 4. Independent (not on one linear line) and dependent points



points selected on the LCD, and (X'_1, Y'_1), (X'_2, Y'_2), and (X'_3, Y'_3) are the corresponding points on the touch screen, Equations 1 and 2 can be used to write Equation 3:

$$\begin{aligned} X_1 &= \alpha_X \times X'_1 + \beta_X \times Y'_1 + \Delta X \\ X_2 &= \alpha_X \times X'_2 + \beta_X \times Y'_2 + \Delta X \\ X_3 &= \alpha_X \times X'_3 + \beta_X \times Y'_3 + \Delta X \end{aligned} \quad \textbf{(3)}$$

$$\begin{aligned} Y_1 &= \alpha_Y \times X'_1 + \beta_Y \times Y'_1 + \Delta Y \\ Y_2 &= \alpha_Y \times X'_2 + \beta_Y \times Y'_2 + \Delta Y \\ Y_3 &= \alpha_Y \times X'_3 + \beta_Y \times Y'_3 + \Delta Y \end{aligned}$$

Equation 3 can be rewritten in matrix form:

$$\begin{pmatrix} X_1 \\ X_2 \\ X_3 \end{pmatrix} = A \times \begin{pmatrix} \alpha_X \\ \beta_X \\ \Delta X \end{pmatrix} \text{ and } \begin{pmatrix} Y_1 \\ Y_2 \\ Y_3 \end{pmatrix} = A \times \begin{pmatrix} \alpha_Y \\ \beta_Y \\ \Delta Y \end{pmatrix}, \quad \textbf{(4)}$$

where

$$A = \begin{pmatrix} X'_1 & Y'_1 & 1 \\ X'_2 & Y'_2 & 1 \\ X'_3 & Y'_3 & 1 \end{pmatrix}.$$

Calibration methods

The three independent calibration points shown in Equation 4 should be sufficient to get the scaling factors required to correct the mechanical misalignment between the touch screen and the system display.

To resolve Equation 4, both sides can be multiplied by the inverse of matrix A to get

$$\begin{pmatrix} \alpha_X \\ \beta_X \\ \Delta X \end{pmatrix} = A^{-1} \times \begin{pmatrix} X_1 \\ X_2 \\ X_3 \end{pmatrix} \text{ and } \begin{pmatrix} \alpha_Y \\ \beta_Y \\ \Delta Y \end{pmatrix} = A^{-1} \times \begin{pmatrix} Y_1 \\ Y_2 \\ Y_3 \end{pmatrix}, \quad \textbf{(5)}$$

where A^{-1} is the inverse of matrix A. The three points—(X_1, Y_1), (X_2, Y_2), and (X_3, Y_3)—are designed/selected on the display surface; and the elements in matrix A are measured from the touch screen during calibration.

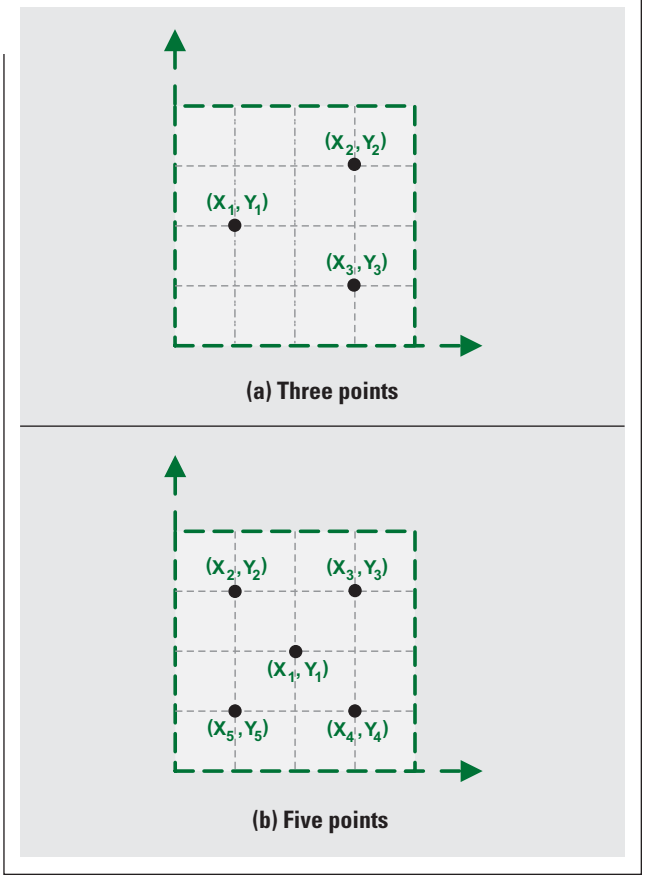
Example 1: Three-point calibration

On a display with 256 × 768 resolution, three calibration points are chosen: (64, 384), (192, 192), and (192, 576). Refer to Figure 5a. During calibration, the three points (678, 2169), (2807, 1327), and (2629, 3367) are measured from a touch panel with 12-bit or 4096 × 4096 resolution. Equation 4 can then be populated with these known values.

$$\begin{pmatrix} X_1 \\ X_2 \\ X_3 \end{pmatrix} = \begin{pmatrix} 64 \\ 192 \\ 192 \end{pmatrix} \qquad \begin{pmatrix} Y_1 \\ Y_2 \\ Y_3 \end{pmatrix} = \begin{pmatrix} 384 \\ 192 \\ 576 \end{pmatrix}$$

$$A = \begin{pmatrix} 678 & 2169 & 1 \\ 2807 & 1327 & 1 \\ 2629 & 3367 & 1 \end{pmatrix}$$

Figure 5. Examples for selecting calibration points



Applying Equation 5 results in $\alpha_X = 0.0623$, $\beta_X = 0.0054$, $\Delta X = 9.9951$, $\alpha_Y = -0.0163$, $\beta_Y = 0.1868$, and $\Delta Y = -10.1458$. Thus the equation for X, from Equation 1, is

$$X = 0.0623 \times X' + 0.0054 \times Y' + 9.9951;$$

and the equation for Y, from Equation 2, is

$$Y = -0.0163 \times X' + 0.1868 \times Y' - 10.1458.$$

In many applications, users may use more than three points in their calibration routines to average or filter the noisy readings from the touch-screen controller. For calibration with n > 3,

$$\begin{pmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{pmatrix} = A \times \begin{pmatrix} \alpha_X \\ \beta_X \\ \Delta X \end{pmatrix} \text{ and } \begin{pmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_n \end{pmatrix} = A \times \begin{pmatrix} \alpha_Y \\ \beta_Y \\ \Delta Y \end{pmatrix}, \quad \textbf{(6)}$$

where A is an n × 3 matrix with n > 3 and rank (A) = 3, or

$$A = \begin{pmatrix} X'_1 & Y'_1 & 1 \\ X'_2 & Y'_2 & 1 \\ \vdots & \vdots & \vdots \\ X'_n & Y'_n & 1 \end{pmatrix}.$$

To resolve Equation 6, both sides can be multiplied by A's pseudo-inverse matrix, $(A^T \times A)^{-1} \times A^T$, where A^T is A's transpose matrix. That is, the unknown variables α_X, β_X, ΔX, α_Y, β_Y, and ΔY are resolved from

$$\begin{pmatrix}\alpha_X\\ \beta_X\\ \Delta X\end{pmatrix} = \left(A^T \times A\right)^{-1} \times A^T \times \begin{pmatrix}X_1\\ X_2\\ X_3\end{pmatrix} \text{ and}$$

$$\begin{pmatrix}\alpha_Y\\ \beta_Y\\ \Delta Y\end{pmatrix} = \left(A^T \times A\right)^{-1} \times A^T \times \begin{pmatrix}Y_1\\ Y_2\\ Y_3\end{pmatrix}. \quad \textbf{(7)}$$

The solution of Equation 7 is the least-square-error estimation[2] of these unknown variables.

Example 2: Five-point calibration

The same system as in Example 1 is used, but five calibration points on the display are chosen: (128, 384), (64, 192), (192, 192), (192, 576), and (64, 576). Refer to Figure 5b. Equation 6 can then be populated with the five points measured from the touch panel: (1698, 2258), (767, 1149), (2807, 1327), (2629, 3367), and (588, 3189).

$$\begin{pmatrix}X_1\\ X_2\\ X_3\\ X_4\\ X_5\end{pmatrix} = \begin{pmatrix}128\\ 64\\ 192\\ 192\\ 64\end{pmatrix} \qquad \begin{pmatrix}Y_1\\ Y_2\\ Y_3\\ Y_4\\ Y_5\end{pmatrix} = \begin{pmatrix}384\\ 192\\ 192\\ 576\\ 576\end{pmatrix}$$

$$A = \begin{pmatrix}1698 & 2258 & 1\\ 767 & 1149 & 1\\ 2807 & 1327 & 1\\ 2629 & 3367 & 1\\ 588 & 3189 & 1\end{pmatrix}$$

Using Equation 7 provides a solution similar to that found in Example 1:

$X = 0.0623 \times X' + 0.0054 \times Y' + 10.0043$, and

$Y = -0.0163 \times X' + 0.1868 \times Y' - 10.1482$.

Calibration algorithms

To perform these calibration methods in an embedded system, the linear algebra equation set, Equation 4 or Equation 6, must be resolved. The solution can be derived simply from Cramer's rule: For the linear equation set $b = A \times x$, b is a known real vector equal to $(b_1, b_2, \ldots, b_n)^T$; A is a known real, square, full-rank matrix; and x is an unknown real vector equal to $(x_1, x_2, \ldots, x_n)^T$. The unknown elements in x can be calculated by $x_1 = \Delta_1/\Delta$, $x_2 = \Delta_2/\Delta$, . . . , $x_n = \Delta_n/\Delta$, where Δ is the determinant of matrix A, det(A); $\Delta_k = \det(A_k)$ for k = 1, 2, . . . , n; and the matrix A_k is the matrix A but with its k*th* column replaced by the vector x.

Three-point calibration algorithm

Assuming that the dimension of A is 3 × 3, Equation 8 can be determined from Equation 4, based on Cramer's rule:

$$\alpha_x = \Delta_{x1}/\Delta,\ \beta_x = \Delta_{x2}/\Delta,\ \Delta X = \Delta_{x3}/\Delta,$$
$$\alpha_y = \Delta_{y1}/\Delta,\ \beta_y = \Delta_{y2}/\Delta, \text{ and } \Delta Y = \Delta_{y3}/\Delta. \quad \textbf{(8)}$$

Variables in Equation 8 are defined in the sidebar on page 9.

n-point calibration algorithm

As in Equation 6, it can be assumed that the dimension of A is n × 3 with n > 3. To get the least-square solutions of the linear equation set, Equation 7 must first be rewritten as

$$\begin{pmatrix}\alpha_X\\ \beta_X\\ \Delta X\end{pmatrix} = \mathbf{A}^{-1} \times \begin{pmatrix}\mathbf{X}_1\\ \mathbf{X}_2\\ \mathbf{X}_3\end{pmatrix} \text{ and } \begin{pmatrix}\alpha_Y\\ \beta_Y\\ \Delta Y\end{pmatrix} = \mathbf{A}^{-1} \times \begin{pmatrix}\mathbf{Y}_1\\ \mathbf{Y}_2\\ \mathbf{Y}_3\end{pmatrix}, \quad \textbf{(9)}$$

where $\mathbf{A} = A^T \times A$, $(\mathbf{X}_1, \mathbf{X}_2, \mathbf{X}_3)^T = A^T \times (X_1, X_2, X_3)^T$, and $(\mathbf{Y}_1, \mathbf{Y}_2, \mathbf{Y}_3)^T = A^T \times (Y_1, Y_2, Y_3)^T$. Then, based on Cramer's rule, Equation 10 can be determined:

$$\alpha_x = \Delta_{x1}/\Delta,\ \beta_x = \Delta_{x2}/\Delta,\ \Delta X = \Delta_{x3}/\Delta,$$
$$\alpha_y = \Delta_{y1}/\Delta,\ \beta_y = \Delta_{y2}/\Delta, \text{ and } \Delta Y = \Delta_{y3}/\Delta, \quad \textbf{(10)}$$

where

$$\Delta = n \times \left(a \times b - c^2\right) + 2 \times c \times d \times e - a \times e^2 - b \times d^2,$$
$$\Delta_{x1} = n \times \left(\mathbf{X}_1 \times b - \mathbf{X}_2 \times c\right) + e \times \left(\mathbf{X}_2 \times d - \mathbf{X}_1 \times e\right) + \mathbf{X}_3 \times \left(c \times e - b \times d\right),$$
$$\Delta_{x2} = n \times \left(\mathbf{X}_2 \times a - \mathbf{X}_1 \times c\right) + d \times \left(\mathbf{X}_1 \times e - \mathbf{X}_2 \times d\right) + \mathbf{X}_3 \times \left(c \times d - a \times e\right),$$
$$\Delta_{x3} = \mathbf{X}_3 \times \left(a \times b - c^2\right) + \mathbf{X}_1 \times \left(c \times e - b \times d\right) + \mathbf{X}_2 \times \left(c \times d - a \times e\right),$$
$$\Delta_{y1} = n \times \left(\mathbf{Y}_1 \times b - \mathbf{Y}_2 \times c\right) + e \times \left(\mathbf{Y}_2 \times d - \mathbf{Y}_1 \times e\right) + \mathbf{Y}_3 \times \left(c \times e - b \times d\right),$$
$$\Delta_{y2} = n \times \left(\mathbf{Y}_2 \times a - \mathbf{Y}_1 \times c\right) + d \times \left(\mathbf{Y}_1 \times e - \mathbf{Y}_2 \times d\right) + \mathbf{Y}_3 \times \left(c \times d - a \times e\right), \text{ and}$$
$$\Delta_{y3} = \mathbf{Y}_3 \times \left(a \times b - c^2\right) + \mathbf{Y}_1 \times \left(c \times e - b \times d\right) + \mathbf{Y}_2 \times \left(c \times d - a \times e\right); \text{ and}$$

$$a = \sum_{k=1}^{n} X_k'^2, \quad b = \sum_{k=1}^{n} Y_k'^2, \quad c = \sum_{k=1}^{n} X_k' \times Y_k', \quad d = \sum_{k=1}^{n} X_k', \quad e = \sum_{k=1}^{n} Y_k',$$

$$\mathbf{X}_1 = \sum_{k=1}^{n} X_k' \times X_k, \quad \mathbf{X}_2 = \sum_{k=1}^{n} Y_k' \times X_k, \quad \mathbf{X}_3 = \sum_{k=1}^{n} X_k,$$

$$\mathbf{Y}_1 = \sum_{k=1}^{n} X_k' \times Y_k, \quad \mathbf{Y}_2 = \sum_{k=1}^{n} Y_k' \times Y_k, \text{ and } \mathbf{Y}_3 = \sum_{k=1}^{n} Y_k.$$

Definitions for Equation 8

$$\Delta = \det(A) = \begin{vmatrix} X_1' & Y_1' & 1 \\ X_2' & Y_2' & 1 \\ X_3' & Y_3' & 1 \end{vmatrix} = (X_1' - X_3') \times (Y_2' - Y_3') - (X_2' - X_3') \times (Y_1' - Y_3')$$

$$\Delta_{x1} = \det(A_{x1}) = \begin{vmatrix} X_1 & Y_1' & 1 \\ X_2 & Y_2' & 1 \\ X_3 & Y_3' & 1 \end{vmatrix} = (X_1 - X_3) \times (Y_2' - Y_3') - (X_2 - X_3) \times (Y_1' - Y_3')$$

$$\Delta_{x2} = \det(A_{x2}) = \begin{vmatrix} X_1' & X_1 & 1 \\ X_2' & X_2 & 1 \\ X_3' & X_3 & 1 \end{vmatrix} = (X_1' - X_3') \times (X_2 - X_3) - (X_2' - X_3') \times (X_1 - X_3)$$

$$\Delta_{x3} = \det(A_{x3}) = \begin{vmatrix} X_1' & Y_1' & X_1 \\ X_2' & Y_2' & X_2 \\ X_3' & Y_3' & X_3 \end{vmatrix} = X_1 \times (X_2'Y_3' - X_3'Y_2') - X_2 \times (X_1'Y_3' - X_3'Y_1') + X_3 \times (X_1'Y_2' - X_2'Y_1')$$

$$\Delta_{y1} = \det(A_{y1}) = \begin{vmatrix} Y_1 & Y_1' & 1 \\ Y_2 & Y_2' & 1 \\ Y_3 & Y_3' & 1 \end{vmatrix} = (Y_1 - Y_3) \times (Y_2' - Y_3') - (Y_2 - Y_3) \times (Y_1' - Y_3')$$

$$\Delta_{y2} = \det(A_{y2}) = \begin{vmatrix} X_1' & Y_1 & 1 \\ X_2' & Y_2 & 1 \\ X_3' & Y_3 & 1 \end{vmatrix} = (X_1' - X_3') \times (Y_2 - Y_3) - (X_2' - X_3') \times (Y_1 - Y_3)$$

$$\Delta_{y3} = \det(A_{y3}) = \begin{vmatrix} X_1' & Y_1' & Y_1 \\ X_2' & Y_2' & Y_2 \\ X_3' & Y_3' & Y_3 \end{vmatrix} = Y_1 \times (X_2'Y_3' - X_3'Y_2') - Y_2 \times (X_1'Y_3' - X_3'Y_1') + Y_3 \times (X_1'Y_2' - X_2'Y_1')$$

Algorithm implementation

To implement the preceding calibration algorithms, one of the first tasks after system power up is to develop and run a software routine to perform the following steps:

- Select the display calibration points (X_k, Y_k) for k = 1, 2, . . . , n and n ≥ 3.
- Call the touch-screen controller function to access touch-screen data.
- Touch the first point (X_1, Y_1) on the display, acquire data from the touch-screen controller, and save the touch coordinates (X_1', Y_1').
- Repeat the previous step to get all (X_k', Y_k') for k = 2, 3, . . . , n and n ≥ 3.
- Call the function to calculate α_x, β_x, ΔX, α_y, β_y, and ΔY—for example, call Equation 10 for five-point calibration.

References

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Document Title	TI Lit. #
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2. Frank L. Lewis, *Optimal Estimation: With an Introduction to Stochastic Control Theory* (John Wiley & Sons, Inc., 1986).	—

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Power-management solutions for telecom systems improve performance, cost, and size

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Deregulation and competition in wire line and wireless infrastructure telecommunications systems have accelerated the need for lower-cost equipment solutions with ever-increasing bandwidth. The challenge of power-management requirements for telecom equipment continues to grow. Increasingly, designers are asked to provide more voltage rails for a variety of digital signal processors (DSPs), field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs), and microprocessors. In short, they are required to generate more voltages, at higher currents, more efficiently, with less noise, in a smaller space. And, if that isn't challenge enough, the solution has to cost less, too!

Deploying access equipment closer to the subscriber requires smaller enclosures (pad and pole mounting) that must survive in a tougher environment. Infrastructure equipment is being designed for smaller footprints, as central office space comes at a premium. Factors driving power management are size, thermal management, cost, and electrical performance (regulation, transient response, and noise generation). This article provides a basic understanding of the evolution of board-mounted power systems, and how the latest generation can achieve higher performance and lower cost—in a smaller footprint.

Size/efficiency/cost

The need to address size, efficiency, and cost simultaneously has ignited renewed interest in power architectures. The first generation of board-mounted power used a power architecture known as a distributed power architecture (DPA) (see Figure 1). This architecture used an isolated (brick) power module for every voltage rail. It worked well when there were limited rails, but cost and PCB space increased significantly with each added voltage rail. Sequencing of the voltage rails also was difficult and required adding external circuitry, which in turn increased cost and board space.

To deal with the size and cost constraints of DPA, second-generation systems moved to a fixed-voltage intermediate bus architecture (IBA) (Figure 2). An IBA uses a single, isolated-brick power module and many nonisolated, point-of-load (POL) DC/DC converters. The POLs can be either power modules, such as the Texas Instruments (TI) PTH series, or discrete buck converters. The isolated converter works over the same input-voltage range as the first generation, either 36 to 75 V or 18 to 36 V. It creates an IBA supply that is regulated to 3.3 V, 5 V, or 12 V. The voltage choice is up to the system designer. This design results in less board space, lower cost, and easier sequencing of the

Figure 1. Typical DPA architecture

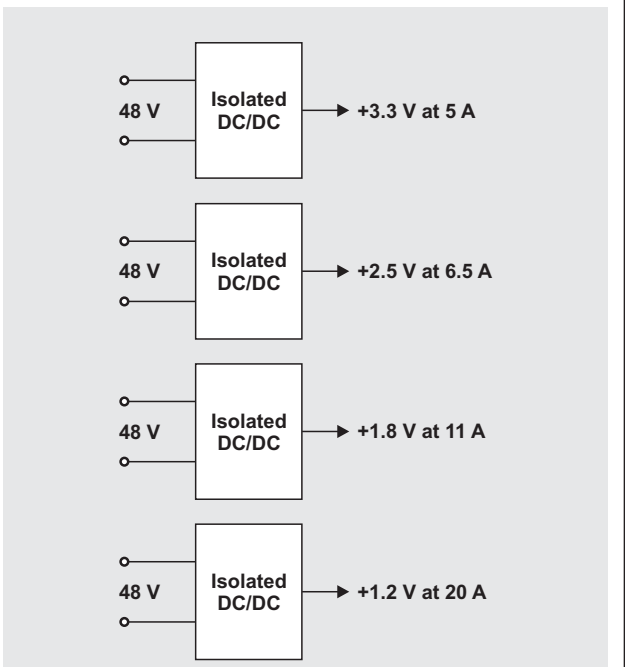
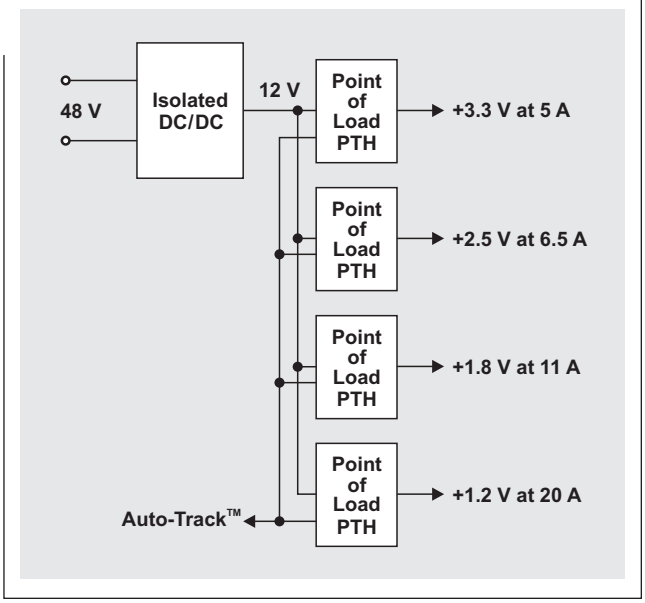


Figure 2. Fixed-voltage IBA



voltages due to features such as TI's Auto-Track™. The only drawback of this architecture is reduced efficiency due to the double conversion required for each voltage.

Today, most telecom systems use a fixed-voltage IBA. However, a higher-efficiency and smaller-footprint solution is needed as access-equipment designs evolve to sealed enclosures with no forced air cooling. As every designer knows, the best way to get rid of heat in a system is not to create it. The main focus for improving efficiency is the front-end isolated converter, since all of the power goes through it. The proven way to increase isolated-converter efficiency is to run the converter at a fixed duty cycle and not regulate the output. This method led to the unregulated intermediate bus architecture (Figure 3).

This architecture uses an unregulated bus converter that creates an output voltage as a ratio of the input voltage. In the example, an ALD17 5:1 converter creates an output voltage that is ⅕ of the input. This technique allows a 150-W system/board to be designed with a 1/16 brick, achieving 96% efficiency for the first conversion stage. Unregulated voltage became possible when wide-input (4.5- to 14-V) PWMs and power modules such as TI's T2 products were introduced. This architecture is limited by the bus converters' maximum input range of 36 to 55 V to keep the input voltage to POLs less than 12 V. The 12-V maximum is necessary because, for POLs to generate output voltages of 1 V or less, the input voltage cannot exceed 10 to 12 times the output. However, an increasing number of telecom original equipment manufacturers (OEMs) are considering a move to this limited input range for the significant cost savings, size reduction, and efficiency improvements obtained with this architecture.

Some telecom OEMs insist on maintaining the traditional, wider input-voltage specification of 36 to 75 V with input transients of up to 100 V. For these requirements, the power industry has responded with the quasiregulated IBA (Figure 4). The main difference between this and the unregulated IBA is that if the input voltage exceeds 55 to 60 V, the quasiregulated IBA regulates the output voltage to around 10 V. The drawback of this approach is that the isolated power module must increase in size to accommodate the regulation circuitry, and its efficiency is reduced when the input voltage exceeds 55 V. An example of this kind of product is the TI PTQB series.

Figure 3. Unregulated IBA

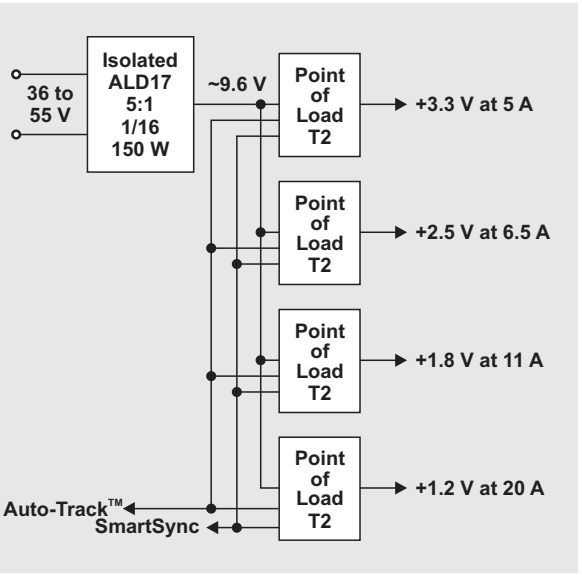
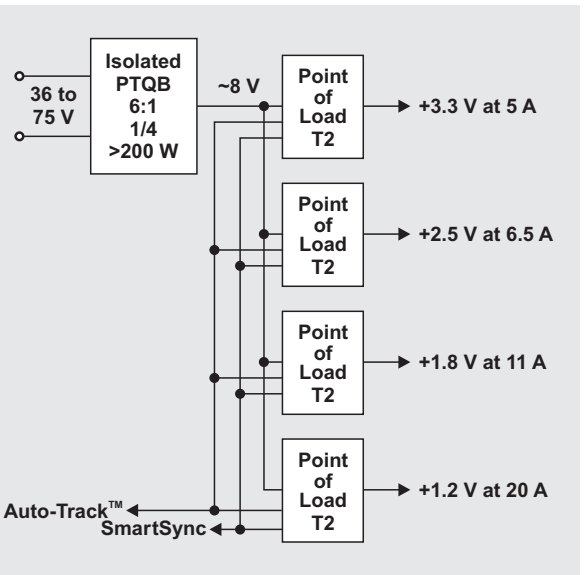


Figure 4. Quasiregulated IBA



Architecture comparison

To provide a meaningful comparison, each example in Figures 2, 3, and 4 has identical output-voltage and current requirements. The examples are based on a theoretical base station utilizing multiple high-performance DSPs with associated analog and digital circuits. The output voltages are 3.3 V at 5 A, 2.5 V at 6.5 A, 1.8 V at 11 A, and 1.2 V at 20 A. For a comparison of the architectures described earlier, see Figure 5. The graphs indicate that the ultimate dream is indeed possible. A quasiregulated or unregulated power system can provide higher efficiency in less space at lower cost. The most notable improvement of the quasi/unregulated IBA over the second-generation, fixed-voltage IBA is efficiency. As shown in Figure 5, power-conversion efficiency increased by almost 7%. This translates to a thermal load reduction of 14 W for a 200-W system.

Power modules were used in these examples because they provide the greatest power density and are the solution of choice at many telecom OEMs. Discrete POLs can be used in all systems to reduce cost, but the board space will increase by a factor of two.

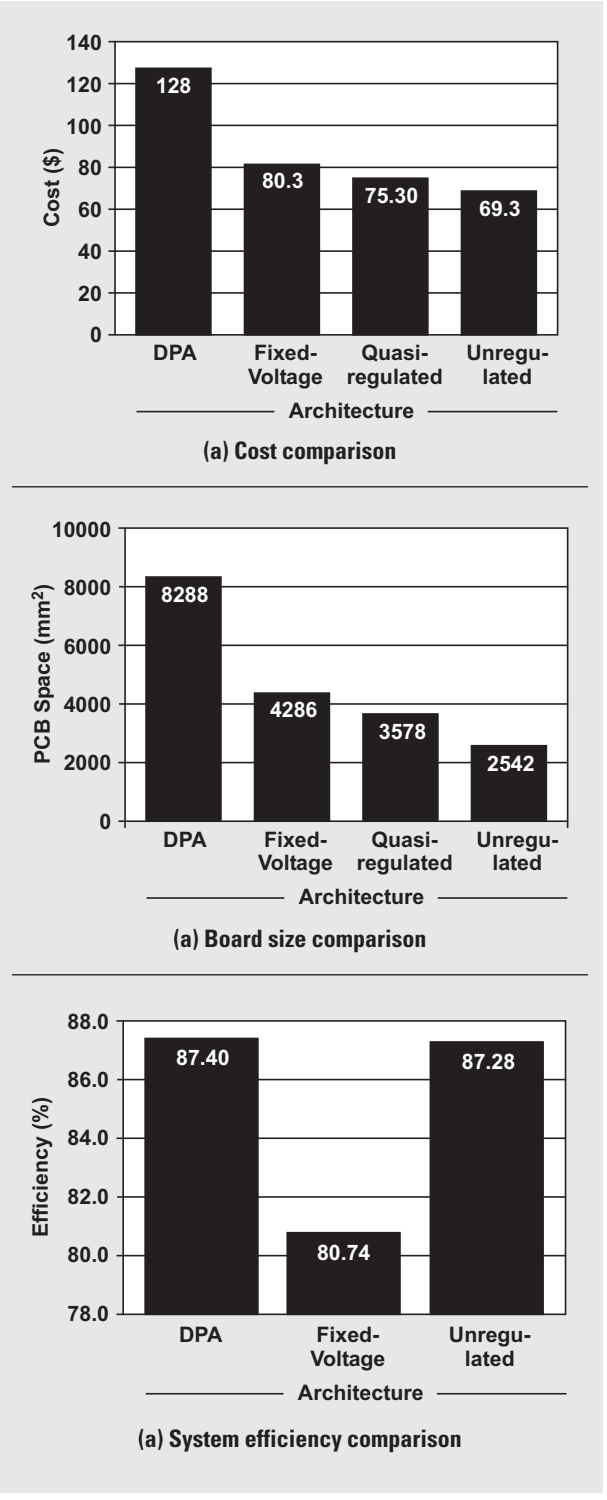
Electrical performance

The remaining challenge for the designer is to meet the increasing electrical demands of the high-performance DSPs and ASICs at the heart of each system. Primary performance issues are voltage regulation, current transient response, and noise.

Regulation and current transient response are closely linked. To get higher performance with lower power in a smaller size, digital semiconductors are fabricated with smaller-geometry transistors that require ever-decreasing voltages. Sub-1-V core-voltage requirements are now becoming the standard. Along with this low voltage have come increasingly tighter tolerances. It is now common practice to specify a total voltage tolerance of 3% that includes line (variations in input voltage), load (small deviations in load current), time, temperature, and current transients. This leaves the power designer with only 30 mV of headroom to accommodate everything the digital system requires. About half of the tolerance budget (15 mV) is usually absorbed by the DC parameters of line, load, time, and temperature. The remaining 15 mV is then available to deal with sudden changes in current (1 to 3 clock cycles) due to computational or data-transmission loads.

This tolerance budget challenges the power-system designer to minimize voltage deviation in the presence of these current transients. If the core voltage (V_{CC}) exceeds the specified tolerance limits, the digital IC may initiate a reset or have logic errors. To prevent this, designers need to pay close attention to the transient performance of the

Figure 5. Comparison of architectures



POL modules being used. Digital loads such as the latest gigahertz DSPs require extremely fast transient responses with very low voltage deviation. To achieve these targets, many additional output capacitors are usually added to the DC/DC converter to provide hold-up time until its feedback loop can respond. The power module, including this added capacitance to meet transient-voltage tolerances, represents the complete power solution.

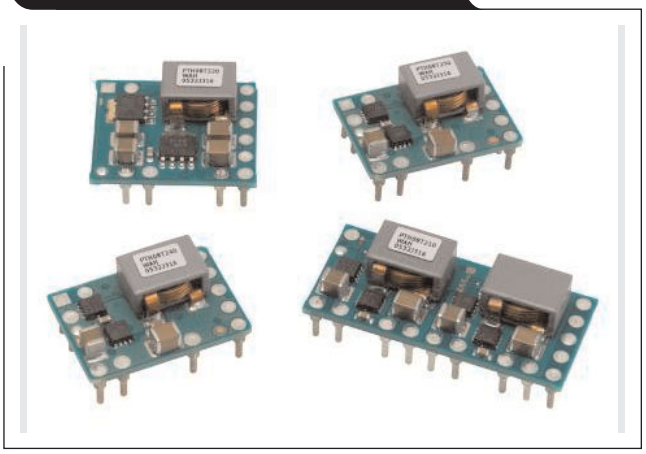
Capacitors have been evolving over the years, with volumetric efficiencies getting better all the time. Even with higher volumetric efficiency, the overall power solution can be over twice the size of the power module alone. This requires a large allocation on the PCB that is usually not available in today's physically smaller systems. What's more, the cost of power-supply materials can be more than double the cost of the power module when the cost of capacitors is added in.

With innovations in DC/DC power-module technology, system designers now are able to achieve faster transient response and less voltage deviation while using less output capacitance. An example is the T2 series next-generation PTH modules (Figure 6) from TI. These devices incorporate a new patented technology called TurboTrans™ that allows custom tuning of the module to meet a specific transient-load requirement. Tuning is accomplished with a single external resistor.

TurboTrans can achieve up to an eightfold reduction in output capacitance, which lowers the cost of capacitors and saves PCB space. Another benefit of this technology is that using a capacitor with ultralow equivalent series resistance (ESR) provides enhanced module-circuit stability. These newer Oscon, polymer-tantalum, and ceramic output capacitors have the additional benefit of being able to withstand high-temperature, lead-free soldering processes.

The final performance hurdle for isolated and POL converters is noise. When switching POLs run at different frequencies and share a common input bus, frequencies resulting from the sum and difference of those frequencies can create beat frequencies that make EMI filtering difficult.

Figure 6. T2 series power modules with TurboTrans™



As an example, if a system has two POLs with one operating at 300 kHz and a second at 301 kHz, the beat frequency is 1 kHz. This can require larger, more complex system filters. T2 power modules from TI have a SmartSync feature that lets the designer synchronize the switching frequency of multiple T2 modules to a specific frequency, which eliminates beat frequencies and makes EMI filtering easier. SmartSync can be used to set the frequency so that switching noise is minimized in a particular frequency band (i.e., xDSL transmission frequencies). TurboTrans and SmartSync are standard features on T2 power modules that add no additional cost to the systems described earlier.

A telecom system built with state-of-the-art power modules allows the system designer to reduce system size, decrease dissipated power, meet the power demands of high-performance digital circuits, and reduce the cost of power compared to regulated-voltage IBA systems.

Related Web site

power.ti.com

TPS6108x: A boost converter with extreme versatility

By Jeff Falin
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Introduction

The TPS61080 and TPS61081 are highly integrated boost converters that have adjustable outputs of up to 27 V with input voltages as low as 2.5 V. The difference between the two versions is the current-limit rating of the integrated power switches (typically 0.5 A and 1.3 A, respectively). The TPS6108x boost converters have a traditional current-mode-control scheme and a constant pulse-width-modulation (PWM) frequency for low-noise operation. The switching frequency can be configured to either 600 kHz for light-load efficiency or 1.2 MHz for smaller, external components. With integrated feedback compensation, internal power switches, and fast PWM switching, the 3 × 3-mm QFN package enables an extremely small boost converter for a wide variety of applications. An example is a 12- or 24-V industrial power rail from a 3.3- or 5-V bus. Additional features include high efficiency, an adjustable reference voltage, and redundant protection circuits—all of which make the TPS6108x ideal for boosting the 3.6-V Li-ion battery voltage used in most portable applications. The converters also support the higher voltages needed for powering thin-film-transistor (TFT) LCDs, OLED displays, WLED backlights, or camera flashlights.

Figure 1. Typical application for a 12-V boosted output

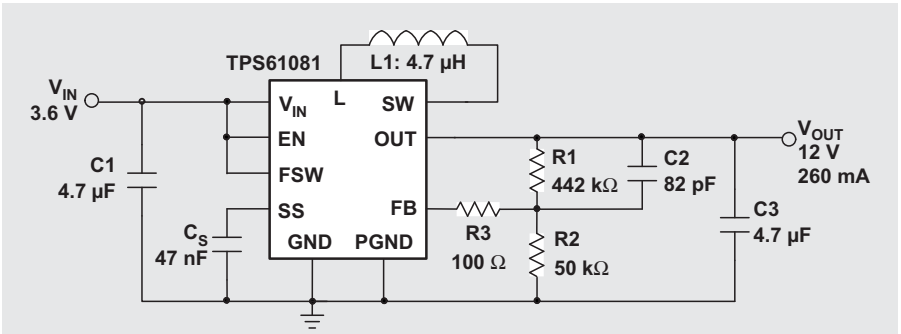
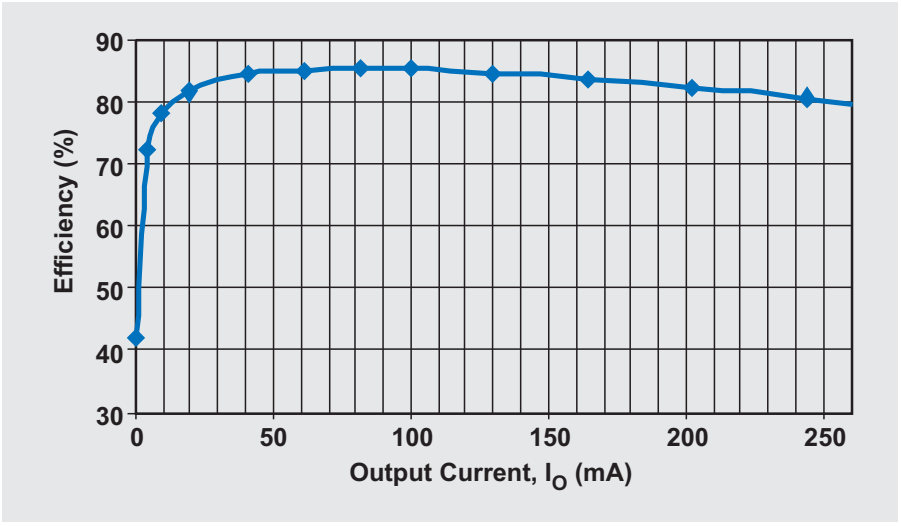


Figure 2. Efficiency with V_{IN} = 3.6 V



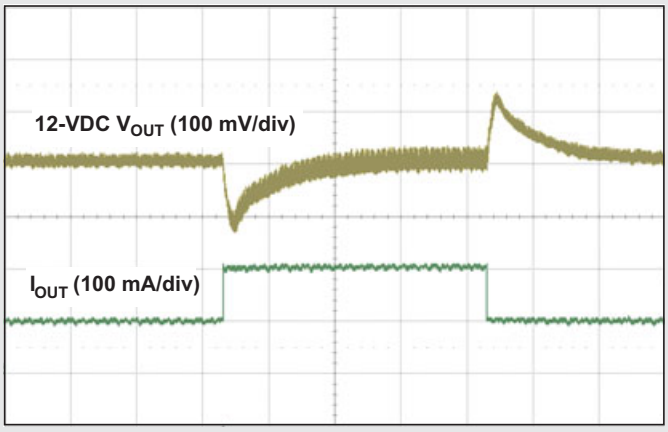
Powering displays

Figure 1 shows the converter in a typical boost configuration that provides a regulated output voltage. When up to 20 V and 100 mA are required to drive each column of a passive-matrix OLED (PMOLED), the 1.3-A switch rating makes the TPS61081 the best choice. When less than 10 V and only tens of milliamps per column for the active-matrix OLED (AMOLED) are provided, the 0.5-A switch rating of the TPS61080 may be more appropriate. In either case, the low-$R_{DS(on)}$ internal switches and the choice of switching frequency provide optimal supply efficiency. Figure 2 shows efficiency data for a 12-V output when a Li-ion battery with a typical 3.6-V source voltage is used.

To support the gates of the TFT drivers for active-matrix LCDs or OLED displays, the high-voltage rail must be capable of fast transients. The TPS61080 has current-mode control and optimized internal compensation; and it can operate at 1.2 MHz with a 4.7-µH inductor, making it ideal

for fast-transient response. Figure 3 shows the transient response of the TPS61080, which was configured as shown in Figure 1 except for an additional 4.7-µF output capacitor.

Figure 3. Transient response of TPS61080



WLED-display backlight driver

As shown in Figure 4, most boost converters can be used to power WLEDs if the voltage-feedback network is replaced with the WLED strings and a series current-sense resistor, R3. The TPS6108x can be used to drive several series WLEDs in parallel for backlighting larger displays.

The voltage across the current-sense resistor is fed back to provide regulation. Traditional boost converters use 1.2-V feedback voltages; therefore, the power loss due to R3 is $P_{LOST} = I_{WLED}^2 \times R3 = 1.2\ V \times I_{WLED}$. The TPS6108x converters have an SS pin that is used to provide variable soft startup for boosted voltage-regulation applications. The SS pin can also be used to lower the FB-pin reference voltage and to reduce sense-resistor power loss in a WLED current-regulation application. Simply connecting a resistor, R1, from the SS pin to GND will lower the FB-pin reference voltage. The reference voltage equates to the resistance of R1 times the SS-pin bias current (I_{SS} = 5 µA typical), resulting in the WLED current calculation:

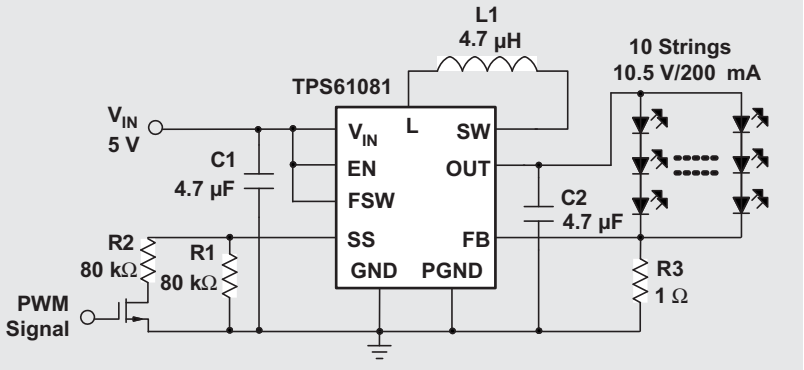
$$I_{WLED} = \frac{I_{SS} \times R1}{R3}$$

A second resistor, R2, in series with the FET and Q1 and in parallel with R1 provides analog dimming by lowering the regulated FB-pin voltage across the sense resistor.

Protection

Two of the most common boost-converter design challenges are how to handle the conduction path from input to output and how to prevent overvoltage. The conduction path creates three problems: leakage voltage under shutdown, inrush current during startup, and excessive short-circuit current. To address these issues, the TPS6108x has an integrated isolation switch that opens during shut-down mode to prevent a possible current path. This isolation switch and the soft-start circuitry also control inrush current during startup to prevent the input supply from drooping and possibly causing system instability. The TPS6108x keeps the isolation FET off until the EN pin is pulled high and V_{IN} rises above the undervoltage-lockout threshold. The Vgs of the isolation FET is clamped so that its high on-resistance limits the inrush current related to charging the output capacitor to V_{IN}. When the output capacitor reaches V_{IN}, the IC fully turns on the low $R_{DS(on)}$ isolation FET and activates soft start as programmed by the soft-start capacitor on the SS pin. In the event that V_{OUT} stays below V_{IN} for more than 2 ms, indicating a short-circuit condition, the isolation

Figure 4. TPS61081 WLED backlight driver circuit



FET turns off and the IC will not restart until the EN pin toggles or V_{IN} goes through power-on reset (POR).

The TPS6108x also has pulse-by-pulse overcurrent limiting, which turns off the power switch once the inductor current reaches a preset value (0.7 A for the TPS61080 and 1.6 A for the TPS61081). The power switch turns back on at the beginning of the next switch cycle. When the inductor current stays above the short-circuit current limit for more than 13 µs or the V_{OUT}-pin voltage goes 1.4 V below V_{IN}, the IC assumes that there is a short-circuit condition and turns off the isolation FET. After 57 ms, the IC attempts to restart. If a momentary short is cleared, the output returns to its regulation voltage and switches normally. For a permanent short, the isolation FET turns off again and waits for POR or EN-pin toggling. Although the isolation switch has a low $R_{DS(on)}$ for minimum power loss, shorting the V_{IN} and L pins can bypass the switch and further enhance the efficiency.

When the TPS61081 is configured for regulated current output as shown in Figure 4, the output voltage could run away if the output impedance becomes too high (i.e., if a WLED burns out or the load is disconnected). To prevent the power switch from exceeding its maximum voltage rating, the overvoltage-protection (OVP) circuit turns off the power switch when the output voltage exceeds the OVP threshold. When the output voltage falls below the OVP threshold, the converter resumes normal PWM operation.

Conclusion

This extremely versatile, integrated-FET boost converter is ideal for industrial, medical, telecom, and consumer applications that require boosted voltages. Features such as variable-reference voltage and multiple-protection circuitry make the TPS6108x also well-suited for powering LCDs and OLED displays.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "High Voltage DC/DC Boost Converter with 0.5-A/1.3-A Integrated Switch," TPS61080/1 Datasheet	slvs644

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS61080
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Get low-noise, low-ripple, high-PSRR power with the TPS717xx

By Jeff Falin
Senior Applications Engineer

Introduction

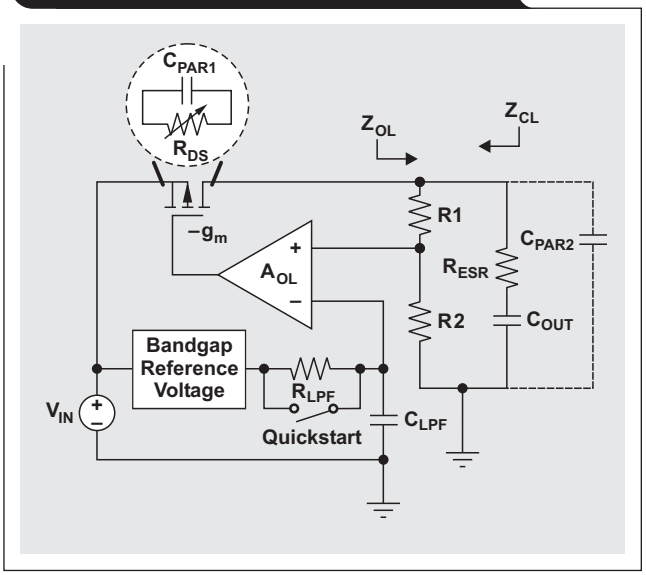
While highly efficient switching power supplies are commonly used for long battery life in portable end equipment such as mobile phones and PDAs, the internal circuitry of some of these devices is sensitive to noise and therefore does not operate properly when powered from a switching power supply with output ripple. Audio circuitry, PLLs, RF transceivers, and DACs are just a few examples of such circuits. Linear regulators are ideal for powering these circuits.

Figure 1 shows a simplified block diagram of a linear regulator using a p-channel MOSFET (pFET) as a pass element. A_{OL} is the open-loop gain of the error amplifier, and g_m is the pass-element transconductance. The error amplifier controls the voltage at the gate of the pass element so that the current through the FET keeps the output voltage regulated relative to the internal reference voltage. Assuming that the low-pass filter (LPF) formed by R_{LPF} and C_{LPF} eliminates nearly all internal-reference noise, the output voltage should be ripple- and noise-free for frequencies within the bandwidth of the regulator's control loop. The concept is easy to understand, but achieving a high power-supply rejection ratio (PSRR) over a wide bandwidth with very low quiescent current and in a small package requires innovative circuits. This article highlights the TPS717xx single-output linear regulator, which provides high power-supply rejection (PSR) over a wide bandwidth with very low quiescent current and in a small package. Similar, dual-output versions are available with the TPS718xx and TPS719xx families. This article also provides guidance on component selection and layout techniques for maximizing PSR and minimizing the regulator's self-generated white noise.

What is the PSRR?

The PSRR is a measure of a circuit's PSR expressed as a ratio of output noise to noise at the power-supply input. It provides a measure of how well a circuit rejects ripple at various frequencies injected from its input power supply. In the case of linear regulators, PSRR is a measure of the regulated output-voltage ripple compared to the input-voltage ripple over a wide frequency range and is expressed in decibels (dB). If the pass element in Figure 1 is treated as a variable resistance, R_{DS}, and the error amplifier and bandgap reference are assumed to have been designed to

Figure 1. Simplified block diagram of a linear regulator



minimize pass-through of the input-voltage ripple, then the PSR is simply a voltage divider, expressed as

$$PSR = \frac{Z_{OL} \parallel Z_{CL}}{Z_{OL} \parallel Z_{CL} + R_{DS}}.$$

In this equation, Z_{OL} is the output impedance at the regulator's output, ignoring the effect of the regulator's feedback loop:

$$Z_{OL} = (Z_{COUT} + R_{ESR}) \parallel (R1 + R2) \parallel C_{PAR2},$$

where Z_{COUT} and R_{ESR} are the output capacitor's impedance and equivalent series resistance (ESR), respectively, and C_{PAR2} is the parasitic capacitance of the output components and PCB. Z_{CL} is the impedance looking back into the output of the regulator, including the effect of the regulator's feedback loop:

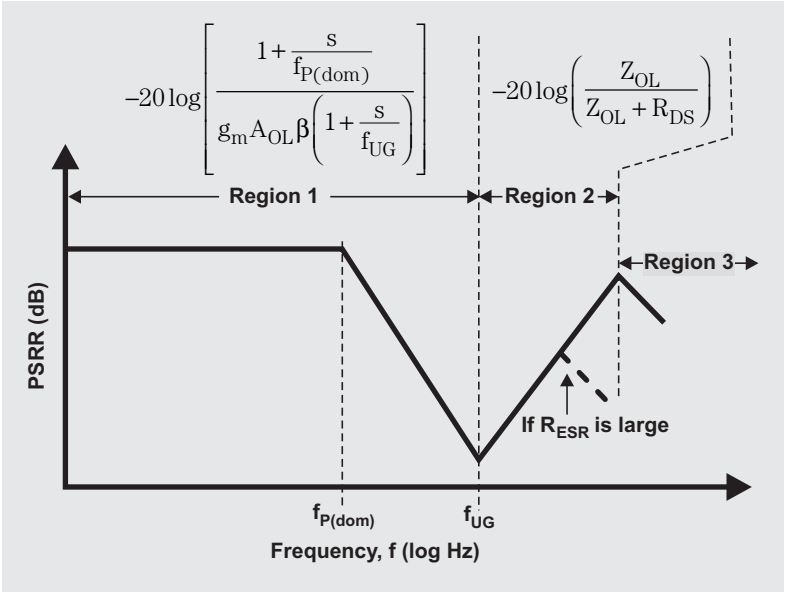
$$Z_{CL} = \frac{Z_{OL} \parallel R_{DS} \parallel C_{PAR1}}{g_m \times A_{OL} \times f \times \beta},$$

where C_{PAR1} is the passive-element parasitic capacitance, f is the ripple frequency, and β is the feedback factor,

$$\beta = \frac{R2}{R1 + R2}.$$

Figure 2 shows the general shape of a PSRR curve, where $f_{P(dom)}$ is the dominant pole and f_{UG} is the unity-gain bandwidth. If the error amplifier is compensated to have a single-pole response, then the Region 1 PSR for amplifier frequencies below f_{UG} can be approximated by the equation on the left side of the graph. Designing the regulator with a high-gain, wide-bandwidth error amplifier can therefore provide high PSR over a wide range of frequencies. In Region 2, above the control-loop bandwidth, the regulator is no longer effective at providing PSR, so the PSRR reduces to a simple voltage divider as shown on the right side of the curve. As Z_{COUT} decreases relative to R_{DS}, the PSR provided by the passive components on the board increases. If C_{OUT} has high R_{ESR}, the PSR peaks sooner. In Region 3, the IC and board parasitic capacitances (C_{PAR1} and C_{PAR2}) dominate, resulting in a capacitive voltage divider, which typically causes the PSR to decrease again. A larger output capacitor with less ESR will typically improve PSRR in this region, but it can also actually decrease the PSRR at some frequencies. This occurs because increasing the output capacitor may lower $f_{P(dom)}$ and/or f_{UG}, depending on how the regulator is compensated, thereby causing the open-loop gain to roll off sooner.

Figure 2. PSRR graph

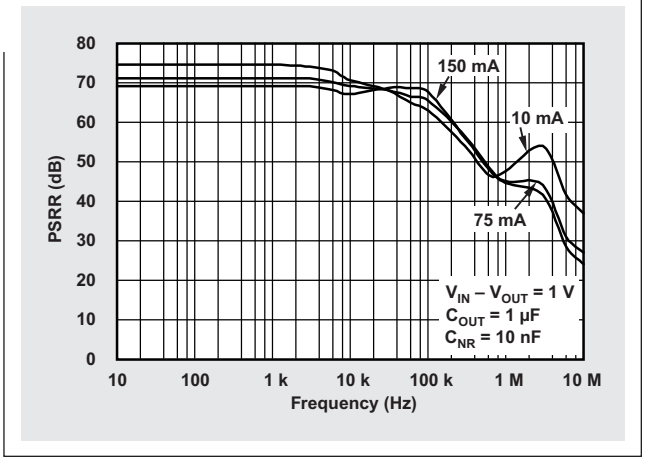


Maximizing PSR

The TPS717xx family of regulators has incorporated both well-known and patentable circuit techniques to provide high PSR over a wide frequency range. An example of the PSRR is shown in Figure 3.

With the simple model previously explained, it can be shown that the TPS717xx's dominant pole with C_{OUT} = 1 µF is at approximately 20 to 30 kHz and the unity-gain frequency is near 400 kHz. Since PSR is a function of the open-loop gain, as the gain varies so will the PSR in Regions 1 and 2 of Figure 2. Figure 3 shows the TPS717xx's PSRR varying with load current. As load current increases, R_{DS} decreases; therefore Z_{CL} decreases, since a MOSFET's output impedance is inversely proportional to its drain current. In many regulators, where $f_{P(dom)}$ varies with Z_{CL}, increasing the load current also pushes $f_{P(dom)}$ to higher frequencies, which increases the feedback-loop bandwidth. As shown in Figure 3, the net effect of increasing the load current is reduced PSRR.

Figure 3. TPS717xx PSRR graph



The differential DC voltage between input and output also affects PSR. As $V_{IN} - V_{OUT}$ is lowered, the pFET (which provides gain) is driven out of the active (saturation) region of operation and into the triode/linear region, which causes the feedback loop to lose gain. Therefore, the PSR of the regulator decreases as V_{IN} approaches V_{OUT}. The lowest PSR, approaching 0 dB, occurs when the device is in dropout ($V_{IN} \approx V_{OUT}$). In this situation, the RC filter formed by the linear regulator's pass-element R_{DS} and output capacitor determines PSR.

Low noise

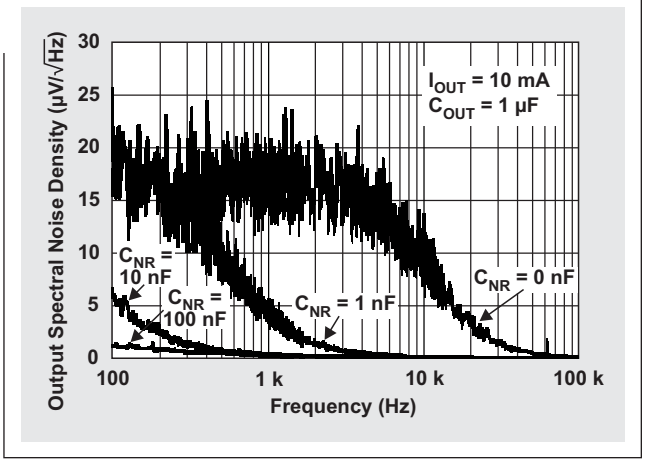
A linear regulator's self-generated noise is sometimes confused with its PSRR. However, noise is generated by the transistors and resistors in the regulator's internal circuitry as well as by the external feedback resistors. Transistors generate shot noise and flicker noise, both of which are directly proportional to current flow. Flicker noise is indirectly proportional to frequency and so is higher at low frequencies. The resistive element of MOSFETs also generates thermal noise like resistors. Thermal noise is directly proportional to temperature, the resistor's resistance value, and the current flow through the transistors. Transistors and resistors closest to the error-amplifier inputs in the small-signal path cause the

most output noise because their noise is amplified by the regulator's closed-loop gain ($A_{CL} = V_{OUT}/V_{Bandgap} = 1/\beta = 1 + R1/R2$). The noise contribution from components later in the signal path is insignificant when compared to the noise at the error-amplifier inputs. In fact, when modest-sized feedback resistors are used, most of the regulator's noise comes from the amplified bandgap reference. As shown in Figure 1, the simplest way to reduce the bandgap noise is to use a low-pass filter (LPF) consisting of an internal resistor, R_{LPF}, and an external capacitor, C_{LPF}. At startup, this filter would slow down the output-voltage rise without the aid of the "quickstart" transistor. When the quickstart transistor is used, it shorts out the R_{LPF} for a short time at startup so the regulator output can rise quickly. Larger noise capacitors such as C_{LPF} in Figure 1 will reduce the output noise produced by the bandgap until the regulator's other noise sources begin to dominate. Using a noise capacitor that is too large results in the quickstart circuit timer expiring before the $R_{LPF} \times C_{LPF}$ time constant. In this case, the output voltage will rise quickly to a level below regulation and then rise very slowly to its final regulated value.

A regulator's noise output is characterized by two measurements. One is its spectral noise density, a curve that shows noise ($\mu V/\sqrt{Hz}$) versus frequency. The other is the RMS of the spectral noise density integrated over a finite frequency range, also commonly called output-noise voltage (μV_{rms}). Figure 4 shows the TPS717xx's spectral noise density with different C_{NR} values, where C_{NR} is the same as C_{LPF} in Figure 1.

When noise specifications of different regulators are compared, it is imperative that the two regulators' noise measurements be taken over the same frequency range and at the same output voltage and current values. When output noise values for regulators at two different output voltages are compared, an approximate noise value can be used that is computed by scaling one of the noise measurements by the ratio of the two output voltages. When a noise-capacitor pin is not available, adding a capacitor across R1 reduces the noise by reducing the closed-loop gain at high frequencies. However, this could potentially slow down start-up time, since the capacitor would have to be charged by the current in the resistor divider; adding such a capacitor could also potentially make the feedback loop unstable.

Figure 4. TPS717xx spectral noise density



Component selection and board layout

Proper board layout and capacitor selection are critical to maximizing PSR and minimizing noise. Low-ESR output capacitors maximize PSR at high frequencies but may increase noise. The reason for this is that the low impedance created by the output capacitor and its ESR may improve stability and PSR by removing peaking in the control loop at frequencies near $f_{P(dom)}$, but removing this peaking would also provide higher gain for the internal noise sources. To maximize PSR and minimize noise, it is recommended that V_{IN} and V_{OUT} have separate ground planes that are connected at the regulator's ground pin. The input, output, and noise-reduction capacitors should be very close to the IC, with the ground of the noise-reduction capacitor as close to the regulator's ground pin as possible.

Conclusion

Linear regulators are ideal for providing a low-ripple, low-noise power rail to sensitive analog circuitry. The TPS717xx single-output and TPS718xx/TPS719xx dual-output linear regulators are specifically designed for providing high PSR over a wide frequency range with low noise. These linear regulators also consume very little quiescent current when powered and even less when shut down, helping maximize battery life in portable powered applications that need bursts of regulator power only at irregular intervals.

References

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3. John C. Teel, "Understanding power supply ripple rejection in linear regulators"	slyt202

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Simultaneous power-down sequencing with the TPS74x01 family of linear regulators

By Jeff Falin
Senior Applications Engineer

Introduction

In the past, ensuring successful power up for DSPs and FPGAs in electronic equipment was a challenge. The most recent DSPs and FPGAs have more relaxed requirements for core and I/O power up/down. However, a few still specify power-up ramp rates and recommend sequential sequencing for predictable and repeatable startup. Even fewer specify power-down requirements, including ramp rates and/or sequences. In most cases, the ultimate goal of these requirements is to ensure that the DSP and FPGA power rails do not have a larger differential voltage than that for which they were designed, even during the brief periods at power up/down. Otherwise, immediate or cumulative damage to internal circuits, which reduces long-term reliability, can occur. Therefore, the ideal method for DSP and FPGA power up/down is for all rails to rise and fall at the same time and rate.

Two or more power-rail ICs are said to have been simultaneously sequenced on power up when they track one another with the same rising dv/dt, and the lower rail stops at its regulated voltage while the upper rail continues to its higher regulated voltage. Various devices, including the TPS74301 linear regulator, have a tracking input to provide simultaneous power-up sequencing. Simultaneous sequencing on power up/down is implemented by replacing the converter's error-amplifier reference voltage with the tracking input signal while the signal is less than the reference voltage. However, for power-down sequencing to work, the converter must have circuitry to pull down the output under light load. Switching converters such as the TPS54x80 family can easily pull down the output by modulating the duty cycle. Most linear regulators do not have pull-down circuitry; so, even though the linear regulator tries to lower the output voltage, it must wait for the output capacitor to discharge through the load resistance. Figure 1 shows a block diagram of the TPS74301 configured to track the 3.3-V rail from a TPS54610. See Reference 1 for a complete schematic of TPS54xxx devices.

Figure 1. Block diagram of TPS74301 providing power-up/down sequencing

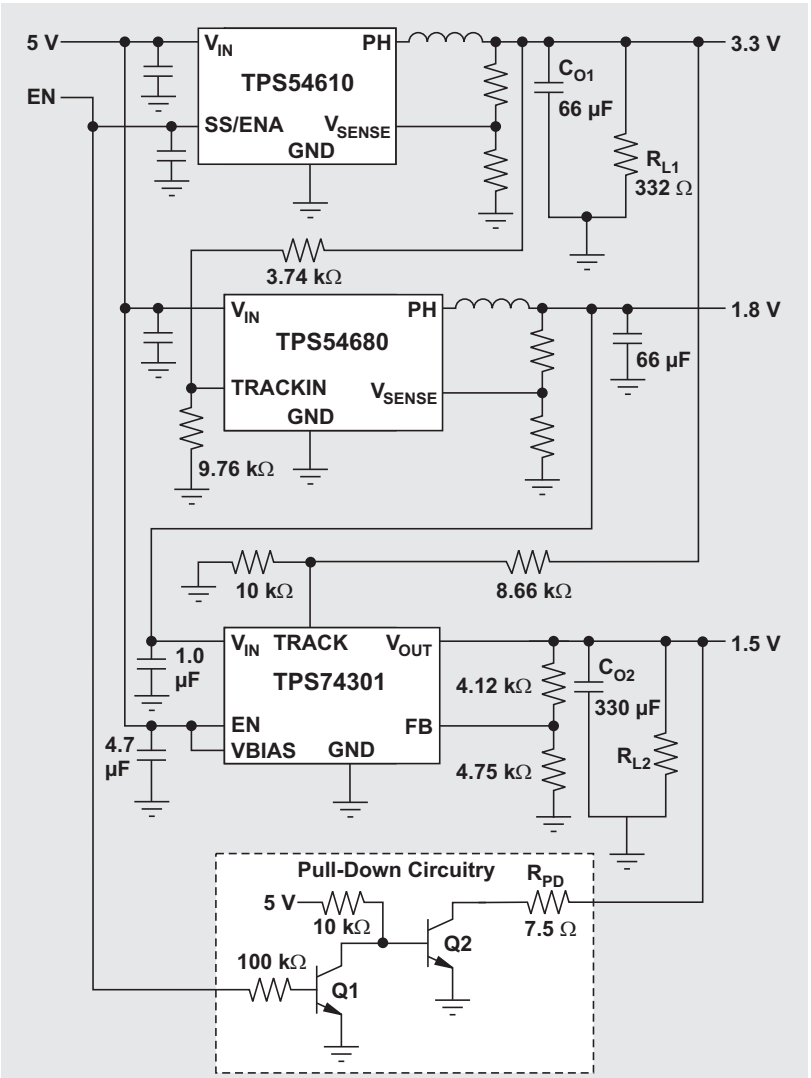


Figure 2 shows simultaneous power up of the 3.3-V and 1.5-V rails. Figure 3 shows that, with the pull-down circuitry (low-cost, bipolar transistors Q1 and Q2 and their supporting components) removed, the TPS74301 output voltage does not track down because the power-down load resistance is too high. The pull-down circuitry shown in Figure 1 adds the pull-down resistor, R_{PD}, in parallel with R_{L2}, which lowers the regulator's load resistance and its RC time constant ($R_{L2} \times C_{O2}$) during power down. This means that the TPS74301 output will track down as shown in Figure 4, since the $R_{PD} \parallel (R_{L2} \times C_{O2})$ time constant is less than the $R_{L1} \times C_{O1}$ time constant.

Figure 2. TPS74301 1.5-V output with power-up sequencing

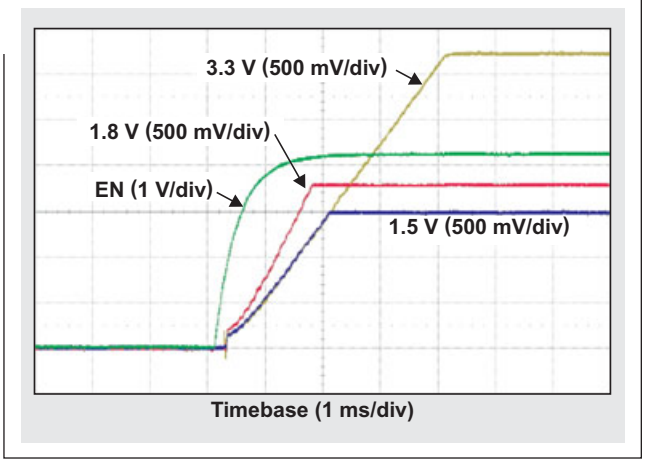


Figure 3. TPS74301 1.5-V output without power-down sequencing

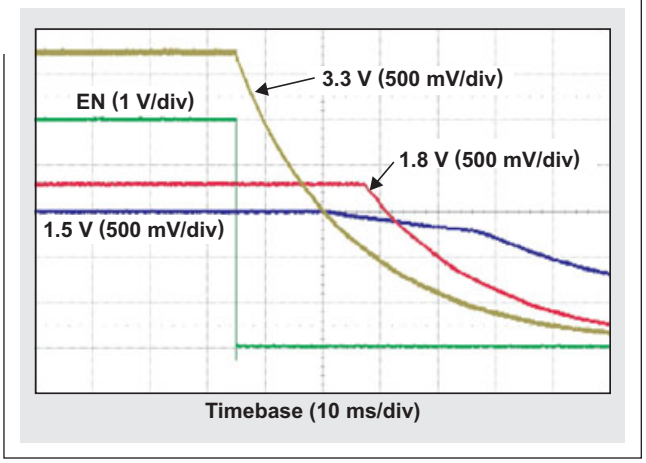
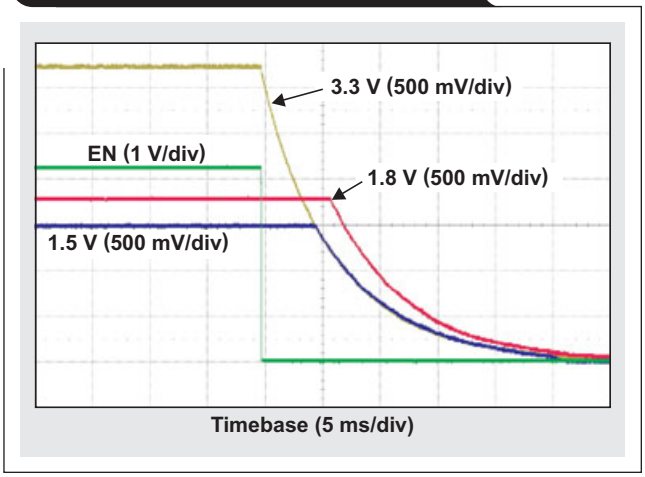


Figure 4. TPS74301 1.5-V output with power-down sequencing



The circuit in Figure 5 shows how to make all versions of the TPS74x01 family achieve "pseudo" simultaneous power-up/down sequencing by having V_{OUT} follow V_{IN}. When V_{IN} is less than the sum of the output voltage and the regulator's dropout voltage (V_{DO}) for a given output load, the regulator's pass element is operating in dropout. Therefore, if the load during power up/down is heavy enough, the regulator's output voltage could be below the voltage being tracked by $V_{DO(max)}$. Note that the soft-start capacitor, C_{SS}, must be set so that the TPS74x01 output ramps up faster than V_{IN}.

Figures 6 and 7 show power-up/down sequencing using the nontracking TPS74801 and TPS74201, respectively, with a 1.5-A output load and V_{OUT} = 1.5 V. Since the TPS74801 has a higher dropout than the TPS74201, the difference between V_{OUT} = 1.5 V and V_{IN} = 1.8 V is more noticeable in Figure 6 than in Figure 7. Figures 8 and 9 show the same results but with no load connected to the output and with V_{OUT} = 1.5 V. Notice in Figures 8b and 9b that on power down the output voltage stays high for a brief time (creating a ledge of sorts) until the pass element's reverse diode turns on to assist in discharging the output capacitance.

Figure 5. Block diagram of TPS74x01 providing pseudo power-up/down sequencing

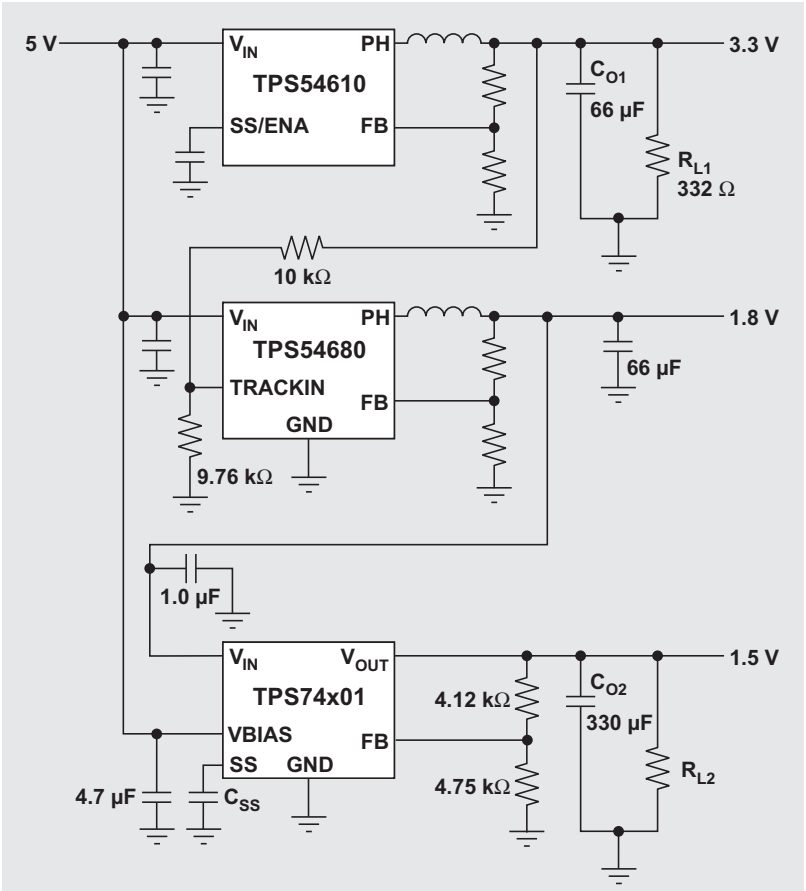
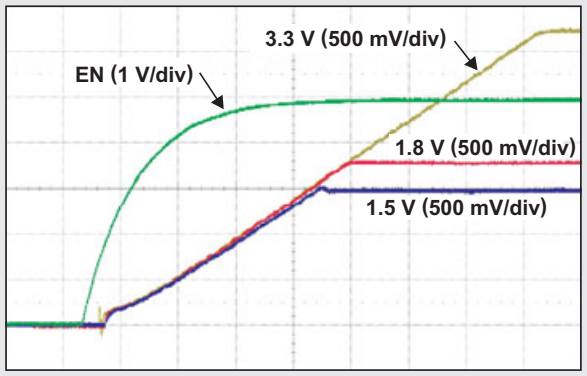
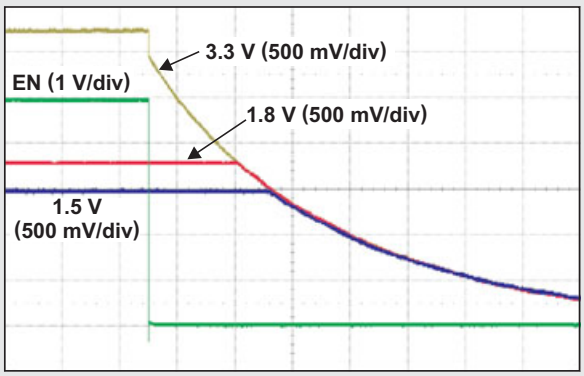


Figure 6. TPS74801 1.5-V output with R_{L2} = 1 Ω

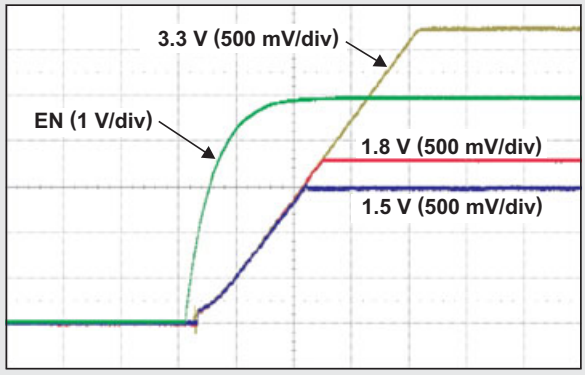


(a) Pseudo power-up sequencing with V_{IN} connected to 1.8-V output

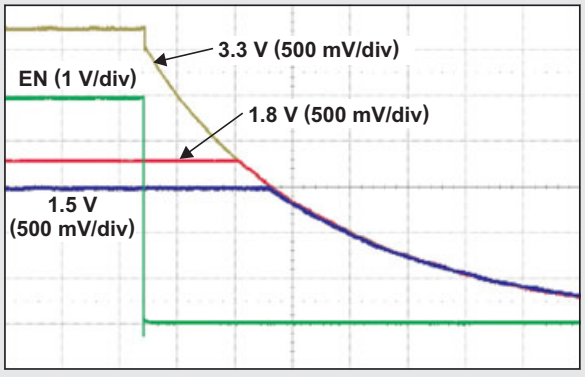


(b) Pseudo power-down sequencing with V_{IN} connected to 1.8-V output

Figure 7. TPS74201 1.5-V output with R_{L2} = 1 Ω

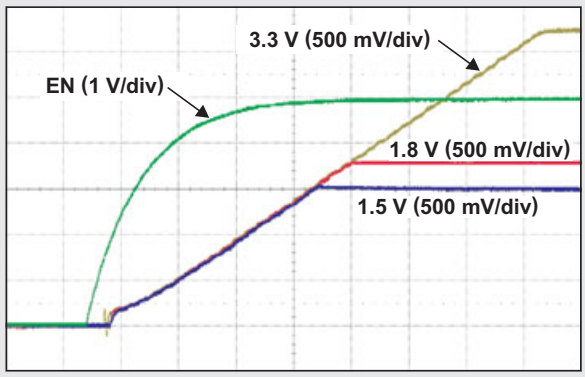


(a) Pseudo power-up sequencing with V_{IN} connected to 1.8-V output

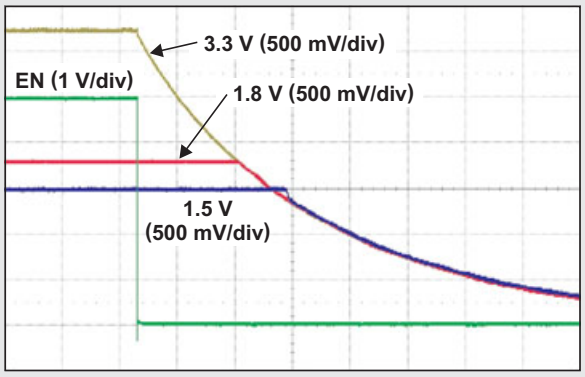


(b) Pseudo power-down sequencing with V_{IN} connected to 1.8-V output

Figure 8. TPS74801 1.5-V output with no load

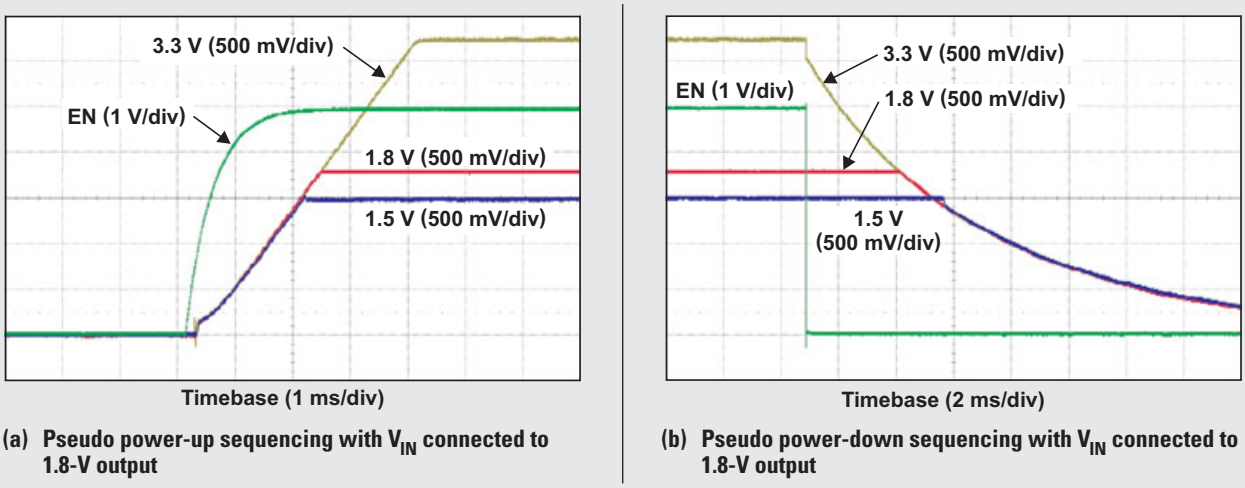


(a) Pseudo power-up sequencing with V_{IN} connected to 1.8-V output



(b) Pseudo power-down sequencing with V_{IN} connected to 1.8-V output

Figure 9. TPS74201 1.5-V output with no load



(a) Pseudo power-up sequencing with V_{IN} connected to 1.8-V output

(b) Pseudo power-down sequencing with V_{IN} connected to 1.8-V output

Conclusion

To meet DSP and FPGA power-on requirements, many new DC/DC converters provide methods for controlling startup. Some also have integrated features to assist with those few DSPs and FPGAs that have power-down requirements. The TPS74x01 family of linear regulators easily provides simultaneous power-up sequencing and, with the assistance of simple pull-down circuitry and/or careful sizing of the load resistance at power down, provides two different methods for achieving simultaneous power-down sequencing.

Reference

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