LM81,LM86,LM87,LM95010

Cost Effective Partitioning of IO and Management Functions in PCs - Introduction of SensorPath?ao Technology

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Technology Edge

Cost Effective Partitioning of IO and Management Functions in PCs - Introduction of SensorPath™ Technology

By Ronnie D. Hughes

Early model personal computers used discrete devices to implement serial ports, parallel ports, keyboard controllers, floppy diskette controllers and other such I/O interfaces. As technological capability increased, the Super I/O (SIO) device integrated these functions into a single device, along with system power shut-down and wake-up control logic. The SIO device has become the catchall logic device where miscellaneous system functions go. It also is used as a device to accommodate "legacy" functions as they move from the system chip set, to the SIO, to extinction. An example is the parallel ATA to serial ATA transition. Chipsets are dropping parallel ATA interfaces. The SIO will provide P-ATA interface for a while until parallel ATA drives are extinct, and then the interface will be dropped.

Processor performance increases have continuously driven power consumption up. This necessitated thermal monitoring and fan control. In some systems, voltage monitoring was also desired. Initially, these functions were implemented with discrete devices such as the LM81, LM86 and LM87 from National, the AD1032 and AD1026 from Analog Devices, and the MAX6656 and MAX6654 from Maxim. These devices communicated over I^2C or SMBus interfaces.1,2 Cost and space reduction goals once again caused designers to look to the SIO as the logical place to integrate this functionality. Monitoring of the CPU remote thermal diode and voltage rails require analog mixed signal circuits. SIO designs converted to mixed-signal circuits and the remote diode temperature interface, analog voltage inputs and the necessary analog to digital converters were integrated into the SIO. An early example of a SIO with integrated health monitoring features was the PC87364 from National. Other SIO manufactures soon followed suit.

Current generation SIO devices use the LPC bus to communicate with the system chipset. Future requirements call for PCI-Express to become the standard intra-system bus. New "legacy" functions moving into the SIO, such as PATA, USB, 1394, as well as expected PCI-E switch functions and PCI-E to PCI bridge functions, are driving the SIO to contain more and more transistors. Smaller and smaller geometries are being used to continue to reduce the cost of the SIO and to provide the necessary switching speeds. Shrinking the geometry of the device is great for the digital portions of the SIO but it has a counterproductive consequence on the analog portions. For a given digital circuit, the required die sizes shrink as geometries are reduced.

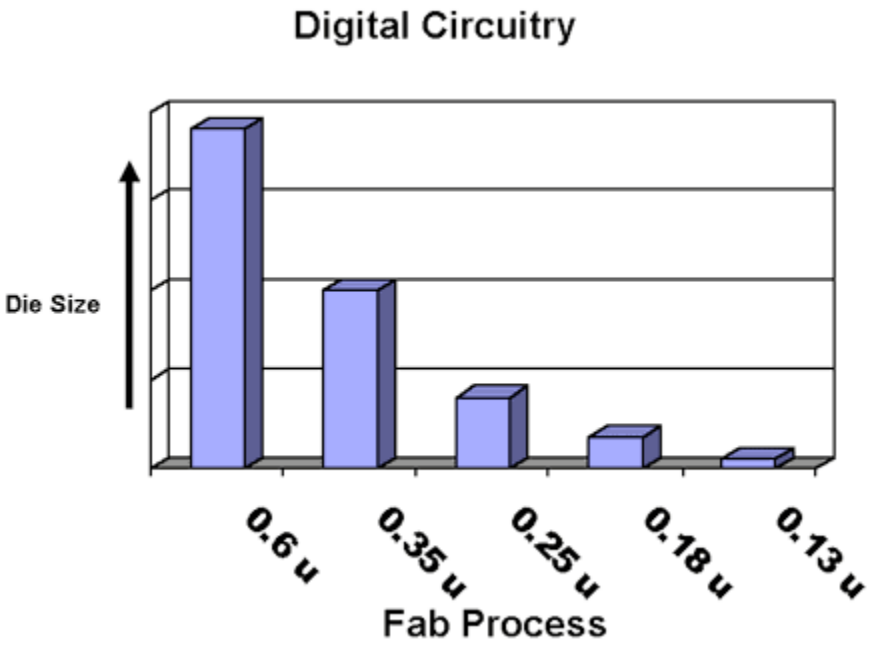


Figure 1. Digital circuit die size is directly proportional to process geometry.

However, for analog circuits below approximately 0.25 microns, the die size required for a given analog circuit does not shrink significantly, and if the same dynamic range performance is maintained, the required die size can actually increase. Substrate noise generated by high-speed digital clocks within a device can also degrade the performance of a sensitive analog device. An example is the remote diode temperature sensor. A change of approximately 241uV represents a 1°C change in temperature.3 High-speed digital switching can readily induce noise of much greater magnitude.

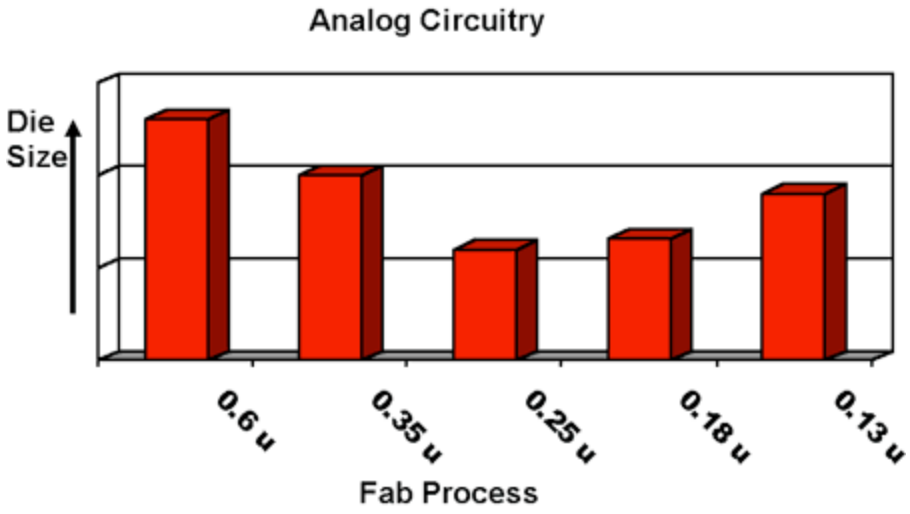


Figure 2. Analog circuit die size does not necessarily decrease with smaller geometries.

Additionally, production test systems for mixed-signal devices are typically slower and more involved than pure digital systems and require more capable test equipment. This increases the cost of SIO devices that have integrated analog circuitry. Location of the SIO on the system board is usually selected based on proximity to the I/O connectors, which are normally on the back panel. In most cases, this results in the SIO being at the opposite side of the board from the analog signals that require monitoring. The result is difficulties in routing the analog signals to the SIO, and the resulting long traces are susceptible to induced noise problems and reduced accuracy.

Integrating system monitoring analog functions in the SIO results in increased device production and testing costs, and increased difficulty of component placement, system layout and signal routing, while producing reduced accuracy and performance. Therefore, a different approach to partitioning the analog and digital portions of the system monitoring features is needed.

One potential solution is to return to the use of I^2C or SMBus discrete sensors. This is possible, but does not provide the optimum results. The I^2C or SMBus interface requires substantial digital circuitry in each sensor and the size and complexity of this circuitry tend to keep the cost of the sensor higher than it would be if a simpler interface were used. Furthermore, software interfaces tend to vary from one device to another with no clear cut standard as to how devices are discovered, identified, configured and used by the system software. Another factor with I^2C and SMBus in real-world systems is noise sensitivity that leads to device lock-up and bus "hangs." This factor is most prevalent when long traces are required between the sensor and the SMBus master and is a particularly troublesome issue when using older sensors because of their general lack of clock filter. Many systems today use multiple I^2C or SMBus segments in order to reduce the number of devices affected if a bus hang occurs. Maintaining signal integrity on I^2C and SMBus has become a real challenge for system designers.

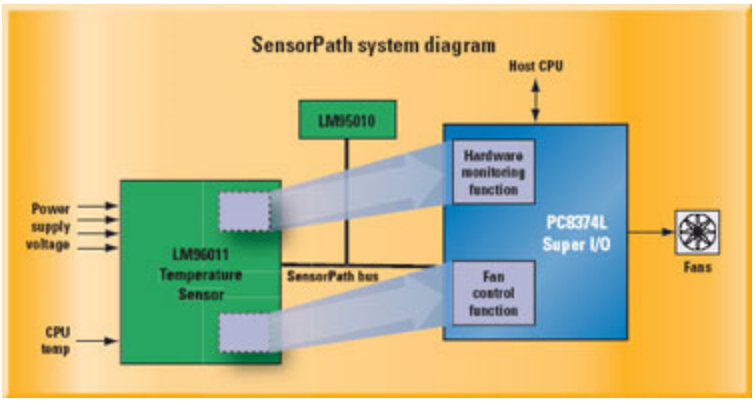
The ideal solution should have the following attributes:

- Analog sensors designed and manufactured on optimum analog process

- Minimum digital logic within the sensor
- Minimum number of signals in the sensor / master interface
- High noise immunity and robust bus recovery mechanism
- Wide selection of devices and capability for system scalability
- Object orientated software structure for device discovery, configuration, and usage
- Industry standard supported by multiple vendors

National Semiconductor realized that a new approach was needed to achieve these objectives and began development work toward this goal. The result is SensorPathTM bus, a sensor interface specification that, along with proper partitioning of functions between sensors and controllers, addresses this need and achieves the above objectives. SensorPath bus is a simple yet robust interface that allows the sensors to be designed and fabricated on an optimized analog semiconductor process while the necessary digital logic to collect, store and make decisions on the data is placed in an all digital component such as a SIO or microcontroller. The PC8374L desktop SIO and the PC87427 server SIO are the first SIO products from National that include the SensorPath interface and master controller.

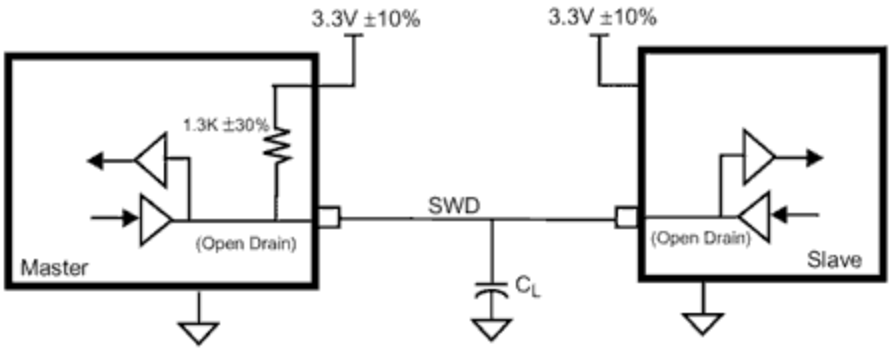
Figure 3. Digital portions of health monitoring hardware should be located in a digital device.



The SensorPath specification allows for two different interface operating modes, asynchronous and synchronous. Asynchronous mode uses a single-wire bus connection between a single master controller, typically located in the SIO, and up to seven slave devices. Synchronous mode adds a clock line to the interface between the master and slaves. Although the specification allows for synchronous mode, asynchronous single-wire mode is considered to be the normal and primary mode, and the mode of interest for this discussion. Therefore, the remainder of this text will discuss only the normal, asynchronous mode of operation.

The Electrical Interface

The electrical component of the specification is designed around a single-wire bus interface that employs a self-synchronizing pulse duration modulation-encoding scheme. The electrical levels are equivalent to SMBus levels; logic low is less than 0.8 volts and logic high is greater than 2.1 volts. An open drain output stage capable of sinking 400ma at a voltage level of 0.4 volts is required at each node. A 0.87KW to 1.625KW pull-up resistor (typically 1.25 KW) is required on the bus and may be supplied by the master or an external pull-up can be used. The timing is based on a 360KHz clock in each node with +-15% tolerance. The pulse width and overall timing tolerances take into account a possible maximum of 30% clock skew between master and slave devices and the effects of driving a 400pF load plus up to 10pF per pin with a 4ma current sink and a 1.625KW pull-up resistor. The rise and fall times are specified at 1000nS and 300nS, respectively.



Bit Signaling and Timing

The bit signaling is via pulse duration modulation. Each bit signal involves driving the signal line to a logic low condition and the duration of the low-level signal on the bus determines which bit signal is being transmitted. Five types of bit signals are defined; Data Bit 0, Data Bit 1, Start Bit, Attention Request, and Reset; these are listed in order of duration from the shortest to the longest as shown in Table 1. The assignment of pulse durations to the bit signals were made to facilitate maximum throughput. Less frequent signals are assigned the longer duration pulses. When no device is signaling on the bus, the signal wire is pulled to a logic high level by the pull-up resistor. The bus is considered idle if no signaling occurs for at least 11 microsecond, TINACT time. A bit signal is initiated when the bus makes a high to low transition, the duration is timed, and the bit signal ends when the bus returns to the high logic level.

Table 1. Bit Signals and Timing Specifications.

Bit Signal	Minimum Time mS	Maximum Time mS
Data Bit 0	11.8	17.0
Data Bit 1	35.4	48.9
Start Bit	80	109
Attention Request	165	228
Reset	354	500 mS (slave only)

Only the bus master is permitted to initiate Data Bit and Start Bit signals. Only the slaves may initiate an Attention Request signal. Normally, this signal is initiated only after the slave has detected an idle bus. However, it is possible that a master could start a Data Bit or Start Bit signal with a slave's Attention Request. In addition, multiple slaves could initiate an Attention Request at the same time. Because of its length, the Attention Request signal will override the timing of any other bit signal except Reset. Therefore, the master and all slaves are able to detect a disrupted Data Bit or Start Bit signal. In this case, the disrupted bits are ignored and must be re-issued by the originator.

The Reset signal may be initiated by either the master or any slave. Following the Reset signal, the master transmits a time-base training sequence. A slave has the option of using this sequence to adjust its internal timing base to meet the +-

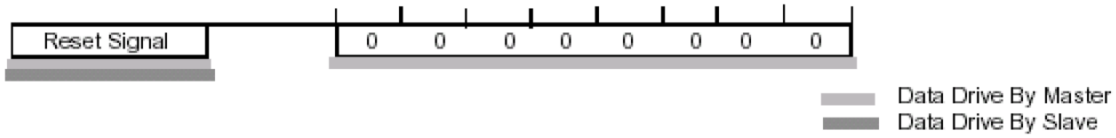
15% clock tolerance, but is not required to do so if the slave's free running clock meets the specification outright. Therefore, the time-base training sequence cannot be used as a means to shift the operating frequency of the slaves to something other than 360 KHz, since not all slaves will implement this option. The maximum switching frequency of the bus is 43.86 Khz when a steady stream of zeroes is transmitted, and decreases as the data content changes.

Bus Transactions & the Message Level Protocol

Only three bus transactions or messages are defined; the Bus Reset transaction, the Read Transaction, and the Write transaction. Only the master initiates a Read or Write transaction while both the master and slaves must initiate a Bus Reset after power up.

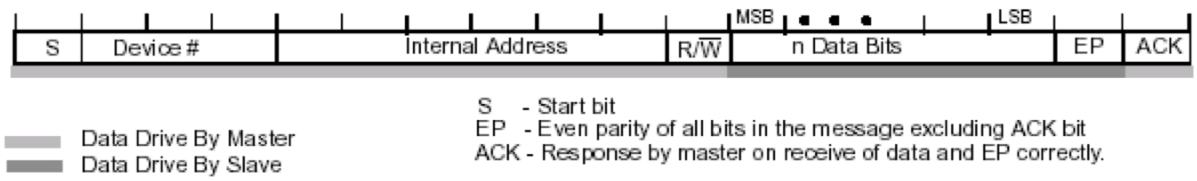
The Bus Reset is the simplest of these three. A Bus Reset must be monitored for and detected by all devices on the bus, and each must reset its communication interface when the signal is received. The device's data register contents are not affected by a Bus Reset, but rather only its communication interface is reset. The master and each slave are required to hold the Bus Reset for at least 354mS after a power-up event. The master may hold the reset signal as long as desired (no maximum) but slaves are required to complete their initialization and release the Reset signal within 500mS of a power-up event. Immediately after the Reset signal is released, regardless of whether it was initiated by the master or a slave, the master must transmit 8 consecutive Data Bit 0 signals to allow the slaves to train their clocks to the master. Notice that no Start Bit signal is transmitted before the eight Data Bit 0 signals.

Bus Reset and Master Driven Clock Training Bit Sequence

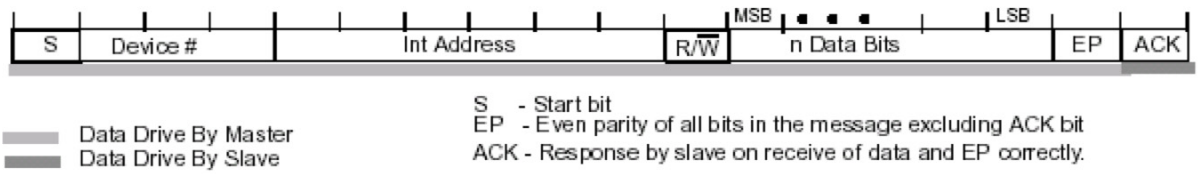


The read and write transactions are very similar, the only difference being the value of the R/W bit and which node is driving the bus during the data bit, even parity and acknowledge bit periods as shown. The even parity bit is calculated across all bits except the start bit, and the acknowledgement bit.

Master Reading Data From A Slave:



Master Writing Data To A Slave:



The three-bit device address allows for seven slave devices on a bus. Device address 0 is reserved for broadcast messages to all slaves. The internal address is a 6-bit field that specifies what register within the slave device is to be read or written.

The message protocol provides positive acknowledgment that a read or write bus transaction completed. A read transaction is "completed" only when the ACK bit is received by the slave. A slave that does not receive a positive ACK bit does not "complete" the transaction, sets its bus error (BER) bit, and then generates an Alert Bit signal. If the master senses a disruption of the ACK bit (a just powered up slave sending a reset for example), the master does not "complete" the transaction either. Normal internal operations in the master are skipped in this case. In either case, the implementation

of the master determines if the transaction will be automatically repeated by the master. The SensorPath specification neither forces nor prohibits automatic retries by the master.

A similar response also occurs when a write transaction fails to receive a positive acknowledgement. If the master does not receive a positive acknowledgement from the slave, it does not complete its internal operations associated with the write transaction. If the slave detects a disruption of the bus while it is generating the ACK bit, it is required to set its BER and generate an Attention Request signal to the master. Again, the implementation of the master determines the automatic retry behavior.

It should now be suspected that the Attention Request signal from the slave is the behavior expected of the slave when a read or write transaction encounters errors. However, if a read or write transaction is in progress, and the master initiates a Start Bit, the slave is required to abort the current transaction and begin the new transaction. In this case, the slave does not initiate an Attention Request. The slave is required to wait indefinitely for a master to send the expected number of bits in a read or write transaction.

Noise Immunity Improvements Over SMBus

The bit signaling and message protocol arrangement of SensorPath bus results in improved noise immunity over SMBus signaling in the following ways:

- A relatively slow 360 KHz internal clock was chosen to reduce the magnitude of noise induced into the sensitive analog circuits.
- The pulse durations are long and the rise and fall times are slow. Glitches on the data bus shorter than a Data Bit 0 signaling period can be ignored. Compare this to a glitch on the SMBus clock line which can clock invalid data into the device. The National Semiconductor implementation of SensorPath devices include a 3 micro-second double sampling filter on the bus data pin, in both master and slave devices.
- The SensorPath pull-up for the high level is of lower impedance: 1.25KW instead of the 8.5KW required by the SMBus specification or the 2.4KW to 4.7KW pull-up typically used on SMBus. Stronger pull-ups are less affected by noise.
- The SensorPath sink current of 4ma is stronger than that of SMBus, which is a minimum of 100mA, and a maximum of 350mA. The stronger output capability allows more bus capacitance to be driven.
- A parity bit is included in the message protocol versus no parity bit in SMBus. Therefore, the parity of the data is checked, rather than just the number of received bits
- The message protocol provides positive acknowledgment that a read or write bus transaction completed. A read transaction is "completed" only when the ACK bit is successfully generated and received.
- The National implementation of SensorPath bus masters in super I/O devices includes additional features to insure robust data transactions and system protection. The master automatically retries failed transactions twice. It verifies each write transaction to a slave device via a read back. Should a sensor read failure occur, the master resets the SensorPath bus and can generate an IRQ, SCI, or SMI to notify the system. Main system power can be turned off by SIO masters after a second read failure of critical sensors, such as those monitoring CPU temperature.

Programming Model

It is somewhat unusual that a bus specification includes a programming model. However, the inclusion of a programming model allows vendors and software developers to work to a common standard. The end result is a higher level of software and device interoperability.

The message protocol section above explained that a three bit device address is used and this allows for seven slave devices on a bus. Device address 0 is reserved for broadcast messages to all slaves. In addition, a 6-bit field in each message specifies what register within the slave device is to be read or written. This addressing scheme allows up to seven devices on each bus segment and up to 64 addressable locations within each device. Table 2 shows the assignment of the 64 available addresses for each device.

Table 2. SensorPath device register address map.

Address Range	Description
0 - 7	Common device registers
8 - 15	Function 1 register set
16 - 23	Function 2 register set
24-31	Function 3 register set
32-63	Reserved address locations

The first eight of these locations are assigned to a fixed set of registers that every slave must implement. These "common" device registers, so called because they are common to every slave device, are described in Table 3. Each slave device can provide from 1 to 3 functions per device and each function is assigned 8 registers locations. The remaining 32 address locations are reserved for future expansion of the specification.

Table 3. Common device register definitions.

Address	Register	Bit Width	Description
0	Device Number	8	A read only register containing the SensorPath device number (address) 1 to 7.
1	MFG ID	16	A read only register containing the manufacturer's ID code as assigned by PCI SIG.
2	Device ID	16	A read only register containing the ID code assigned by the manufacturer to this device. The lower 11 bits contain the ID code and the upper 5 bits contain a revision code.
3	Capabilities – Fixed	16	A read only register containing 3, 4 bit wide fields that identify the 3 possible functions in the device (function descriptors), and a 4 bit field that indicates the size of the optional expansion capabilities register.
4	Device Status	8	A read only register containing the status flags and error flags for each sensor function, and the overall device bus error flag.

5	Device Control	16	A read / write register that contains control bits to enable each of the 3 possible sensor functions, and device level bits to reset, shutdown, and select low power mode operation for the device.
6	Capabilities - Expansion	0, 8, 16, 24, or 32	A read only option register reserved for manufacture specific information about the capabilities of this device. The size of this register is determined by a 4 bit field in register 3.
7	Reserved	NA	Reserved for future expansion of the specification.

Function Descriptors and Registers

The specification defines a 4-bit-wide function descriptor field for each of the three possible functions that a device may contain. A function descriptor value of 0 indicates a non-implemented function. Currently, four non-zero values are defined to provide a temperature measurement function, a voltage only measurements function, a voltage with VID measurement function, and an EEPROM storage function. Four of the remaining function descriptor values are reserved for manufacturer assignment to allow specialized functions and the final four descriptor values are reserved for future use within the specification.

A sensor type function can provide multiple sensor points per function. For example, the temperature measurement function can support up to 7 individual temperature sensors and the voltage measurement functions can support up to 22 voltage inputs. Eight register locations are allocated for each function within a device. The definition for these registers is dependent on the function type, but there is some commonality between the temperature and voltage measurement sensors. Tables 4 and 5 provide a summary of the registers associated with these sensor functions. Many of the terms and definitions are specific to Intel processors and support circuitry, e.g. PROCHOT, VR_HOT, and VID. Refer the to Intel processor datasheets for an understanding of these terms and the function of these signals. Also, refer to the SensorPath specification4 and to the datasheets for SensorPath devices that implement temperature and voltage sensor functions for additional information. The LM95010 (temperature only device) and the LM96011 (temperature and voltage monitoring device) from National Semiconductor are representative examples.5

Table 4. Definition of registers associated with a temperature measurement function.

Address (Function Base +)	Register	Bit Width	Description
0	Capabilities	16	A read only register containing the capabilities of this temperature measurement function, including, the resolution in degrees, the number of significant data bits in the temperature data, a flag indicating if the data is signed or unsigned, a flag indicating the width of the output register (16 or 24), a flag indicating the presence of an internal temperature sensor, bit to indicated how many external temperature sensors are supported, and bits to indicate how many PROCHOT and VR_HOT input signals are supported, if any.

1	Readout	16 or 24	A read only register containing the temperature reading from the sensor most recently scanned. This register also contains bits indicating the number of the temperature sensor the data same from and error and event flags.
2	Control	16	A read/write register containing enable bits for each of the temperature sensors and an attention request enable bit.
3	Status	8	A read only reserved register for future use to contain temperature sensor status information.
4	PROCHOT Select	8	A write register used to select one of 3 possible pairs of PROCHOT/VR_HOT inputs.
4	PROCHOT Read	16	A read register containing bits indicating if a PROCHOT and/or VR_HOT input activated, and if so, the percentage of the programmable window time that the input was active.
5	PROCHOT Control	8	A read/write register used to set the time window over which PROCHOT is measured.
6	PROCHOT Force Active	16	A read/write register used enable the device to force a particular PROCHOT output active and to program the duty cycle of a PWM controller that drives the output. This register is also used to enable a VR_HOT input activation to force a corresponding PROCHOT output PWM activation.
7	Reserved	NA	Reserved for future specification use.

Table 5. Definition of registers associated with a voltage measurement function.

Address (Function Base +)	**Register**	**Bit Width**	**Description**
0	Capabilities	16	A read only register containing the capabilities of this voltage measurement function, including the number of significant data bits in the voltage data, a flag indicating the width of the output register (16 or 24 bits), a field indicating the number of voltage channels (0 – 22

			channels), a bit to indicated if low scan rate mode is supported, bits to indicate how many VID groups are supported, bit to indicate the bit width of the VID input, and a flag to indicate the size of the control register (16 or 32 bits).
1	Readout	16 or 24	A read only register containing the voltage reading from the channel most recently scanned. This register also contains bits indicating the number of the voltage channel the data came from and error and event flags.
2	Control	16 or 32	A read/write register containing enable bits for each of the voltage channels, which channel number is to be used as the starting point for low rate scan, and an attention request enable bit.
3	Status	8	A read only reserved register for future use to contain voltage sensor status information.
4	VID Select	8	A write register used to select which one of 3 possible VID groups supplies information via the VID Read register.
4	VID Read	16	A read register containing the data from the currently selected VID group inputs, and bits indicating which VID group is selected, and if high limit, low limit, or failure errors have occurred.
5	VID Control	16	A read/write register used to configure the voltage window size used for comparison with voltage measurements during dynamic VID / Vcore monitoring modes. The register also contains bits to enable VID support for voltage channels 0, 1 and 2.
6	Reserved	NA	Reserved for future specification use.
7	Reserved	NA	Reserved for future specification use.

Business Considerations:

Many firms require open standards and alternative vendors for many components. National Semiconductor has enlisted the help of the Distributed Management Task Force (DMTF) as an avenue to achieve an open standard and to encourage board industry acceptance. The DMTF is an organization leading the development, adoption, and interoperability of management standards and initiatives for enterprise and Internet environments. SensorPath bus was recently taken in by the DMTF Systems and Devices working group for consideration and is currently under review. In addition, National is providing royalty-free licenses to any vendor interested in developing and producing SensorPath devices today. There is a growing community of vendors and users of SensorPath technology

Summary:

The ever-shrinking digital semiconductor processes are counterproductive to maintaining high- performance and cost-effective analog sensors. Integration of analog sensors into the Super IO or other digital-only component within a computer system is not the optimal way to provide needed analog monitoring. Discrete SMBus or I^2C devices may be used, however they suffer from noise immunity issues. SensorPath technology was developed to provide an optimal solution with low cost and high noise immunity. The functional partitioning, single- wire interface with pulse width data signaling scheme and standardized programming model taken together result in a number of advantages to the users.

Feature	Benefits
Smart partitioning of functions between analog and digital components	• Cost-effective devices and designs • Allows "sprinkling" of sensors around the board as needed
Dedicated single-wire bus for sensors	• Easy to route • No need for long analog traces • Sensors are close to hotspots • Better noise immunity for sensor communications
Optimized solution for sensor applications	• Lower noise, higher measurement accuracy • PC components run closer to rated limits with less guard band necessary
Standardized programming model	• Reduces software development time • Increases software reuse • Ensures software interoperability with multi-sourced devices

References:

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5. LM96010 and LM95010 Datasheets

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