Radiation Report

LMK04832-SEP Single-Event Effects Report

ABSTRACT

The Space Enhanced Plastic (SEP) product LMK04832-SEP (V62P22612-01XE) was tested under heavy ions and monitored for Single-Event Effects (SEE). No incidences of Single-Event Latchup (SEL) and Single-Event Function (SEFI) were detected up to 48 MeV-cm^2/mg. Testing was performed at the highest operating voltage (3.45 V) and temperature (125°C). Single-Event Upsets (SEU) of the clock were detected but not characterized. The SEP family are radiation tested products in plastic packages for space missions with reduced radiation and reliability requirements.

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Trademarks

1 Product Description

The LMK04832-SEP[1] is part of TI's family of Space Enhanced Plastic products[2] released for space missions with reduced radiation and reliability requirements. The device is a JESD204B, JESD204C[3] compliant clock jitter cleaner with two PLL loops – one for jitter cleaning and one for clock generation. The LMK04832-SEP has reduced radiation performance compared to the QML-V option – LMK04832-SP along with a different pinout and electrical performance.

LMK04832-SEP is the generic part number (GPN) for the product. The flight-grade orderable part number is LMK04832MPAPSEP or V62P22612-01XE[4]. A prototype, which does not receive full space-grade processing and testing, LMK04832PAP/EM, can be ordered for engineering evaluation.

Figure 1-1 shows a simplified block diagram of the LMK04832-SEP, and a more detailed block diagram is shown in Figure 1-2. The LMK04832-SEP can provide very low jitter clocking signals up to 3.2 GHz on 14 individually programmable outputs. The device can be configured for operation in dual PLL, single PLL, or clock distribution modes with or without SYSREF generation or reclocking. PLL2 can operate with either internal or external VCOs[1].

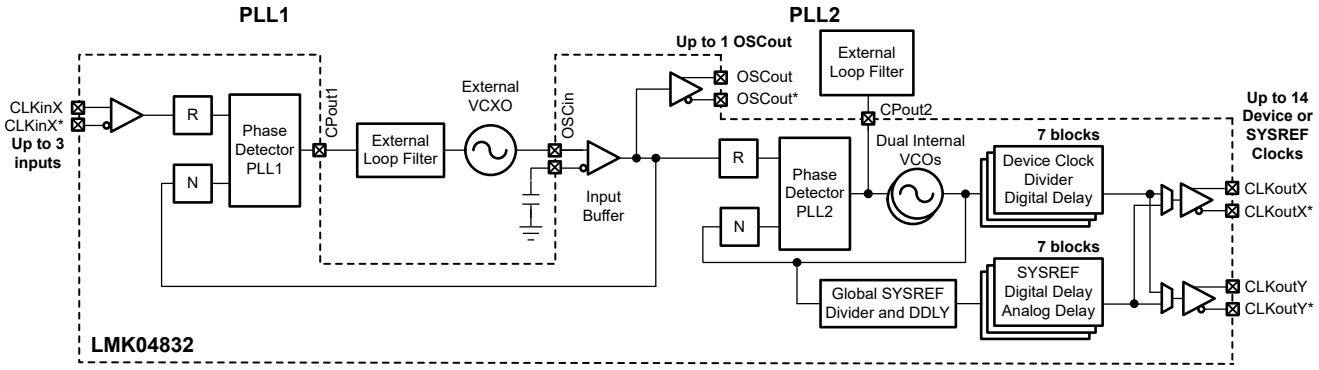

Figure 1-1. LMK04832-SEP Configured in Dual-Loop Mode

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B-compliant data converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. JESD204B is a serial interface standard used between data converters and logic devices with serial data rates up to 12.5 Gbps[4]. SYSREF is a timing phase reference synchronous with the output signal.

Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems. The outputs of the LMK04832-SEP can be individually configured in many different output formats: CML, LVPECL, LCPECL, HSDS, LVDS, or 2 × LVCMOS. The output frequency and delay can be individually set for each output. The product pinout is shown in Figure 1-3.

The part is configured through a serial peripheral interface (SPI) and the configuration is stored in registers. The state of the registers can be accessed through a register read. The operating voltage of the LMK04832-SEP is 3.15 V to 3.45 V.

The LMK04832-SEP is manufactured on a TI BiCMOS process with SiGe NPN bipolar transistors.

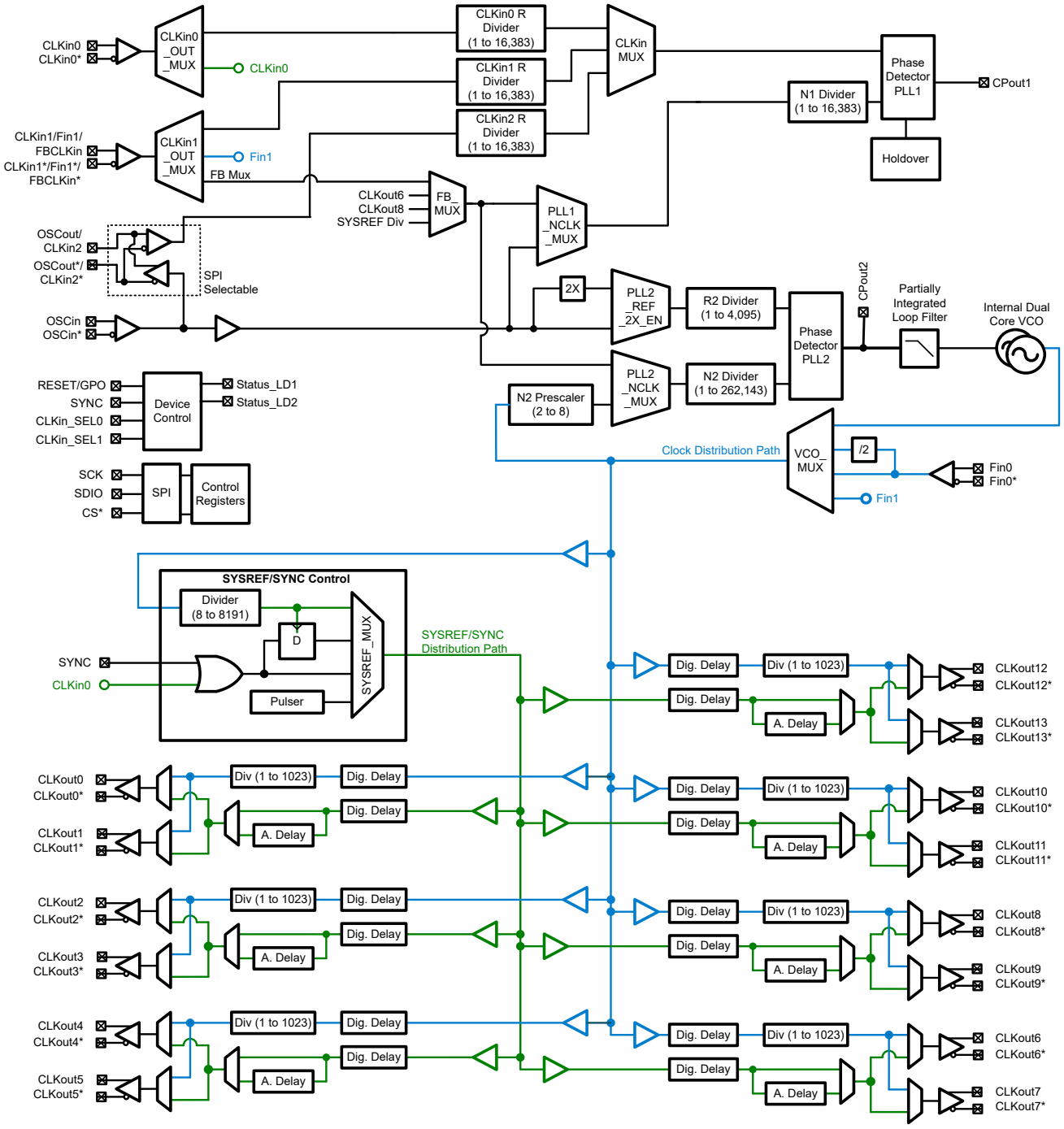

Figure 1-2. LMK04832-SEP Detailed Block Diagram

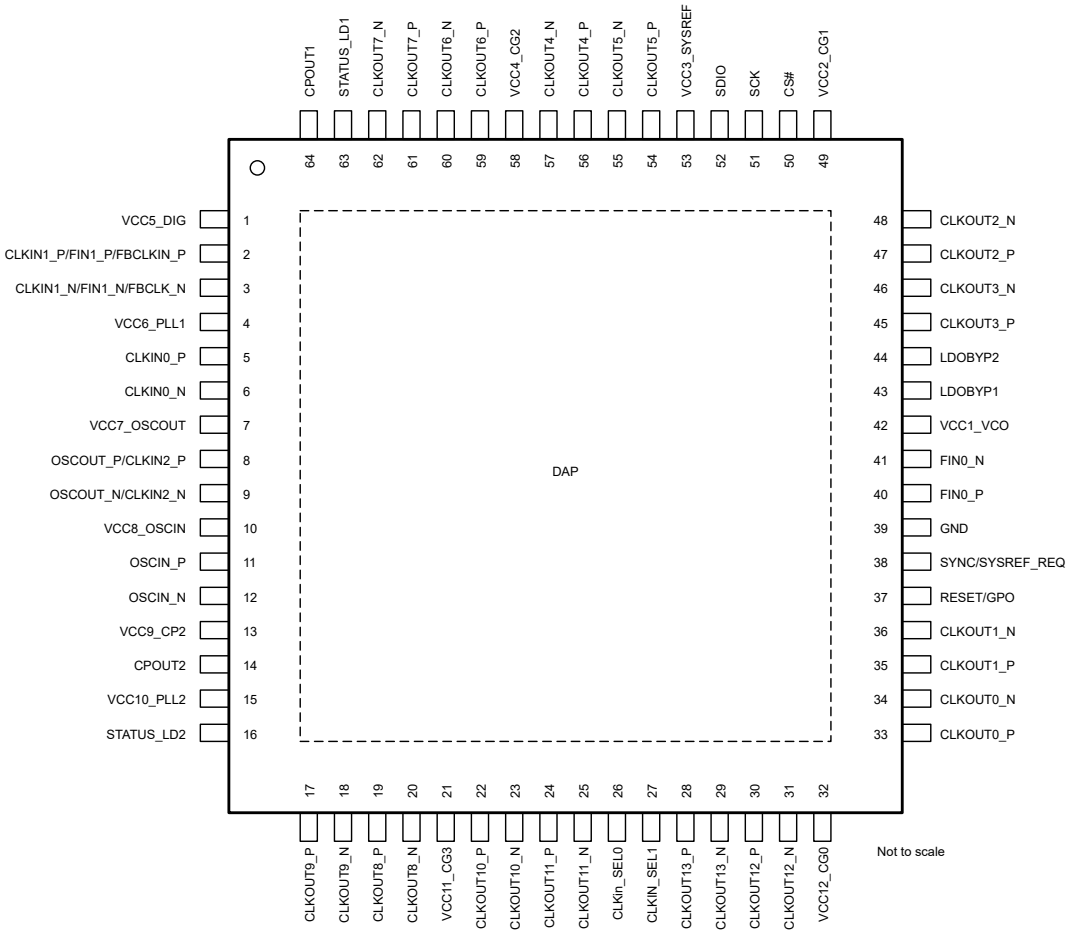

Figure 1-3. LMK04832-SEP Pinout

2 Test Setup

The LMK04832-SEP was monitored for SEL and SEFI, using EIA JESD57 [(5)] as a test guide.

The device under test (DUT) was soldered to a custom evaluation board similar to the LMK04832SEPEVM evaluation board [(6)]. The DUT was decapped to expose the die surface to the ion beam. The active components on the board were bypassed and the power and input signals to the DUT were supplied externally.

Power to the DUT board was supplied by an Agilent 6702 quad supply. The 6702 was controlled and the output current to the DUT board was monitored by an NI-PXIe-8135 controller using a custom LabVIEW™ GUI (PXI Rad Test) developed by Texas Instruments for SEE testing. The voltage was set to 3.45 V as measured at the DUT board.

The DUT was configured with both PLLs enabled. There was a 122.88-MHz signal on PLL1 and a 1.024-MHz signal on PLL2. The internal VCO frequency was set at 2949.12 MHz. All clock outputs were enabled but were configured to different output modes (LVPECL, LVDS, HSDS, CML, and LCPECL) with different dividers and delays so that different functions are tested.

CLKout8 output was monitored with the output in LVDS mode with a Tektronix DPO7354 oscilloscope.

2.1 SEL Test

A thermistor was attached to the DUT board up against the DUT to monitor the temperature. The DUT was heated with a heat gun so that the thermistor read at least 125°C. Based on the power dissipation of the DUT and the thermal modeling of the ceramic package, the junction temperature is approximately 20°C higher than the thermistor reading.

The supply current was monitored on a display in real time and also recorded by the PXI controller.

2.2 SEFI Test

CLKout8 was monitored during the ion run. If the output frequency or amplitude or if the supply current permanently changed and the registers had to be rewritten to return the DUT to the original configuration, this is considered a SEFI.

2.3 Test Facility

Heavy ion irradiation was done using the 15-A MeV cocktail and K500 beam line at the Texas A&M University Cyclotron Institute Radiation Effects Facility (TAMU)[7] on June 2, 2020. The Ag ion was used for a linear energy transfer (LET) of 48 MeV-cm^2/mg to a total fluence of 1.00 × 10^7 ions/cm^2.

3 Results

3.1 SEL Results

SEL was not detected during the ion run. The supply current had some fluctuations due to ion strikes but the variation in current during the ion run was less than 1%. Any momentary increase in current was less than 1 mA. Occasionally the supply current dropped by up to 4 mA but would recover within microseconds. Supply current is plotted in Figure 3-1 .

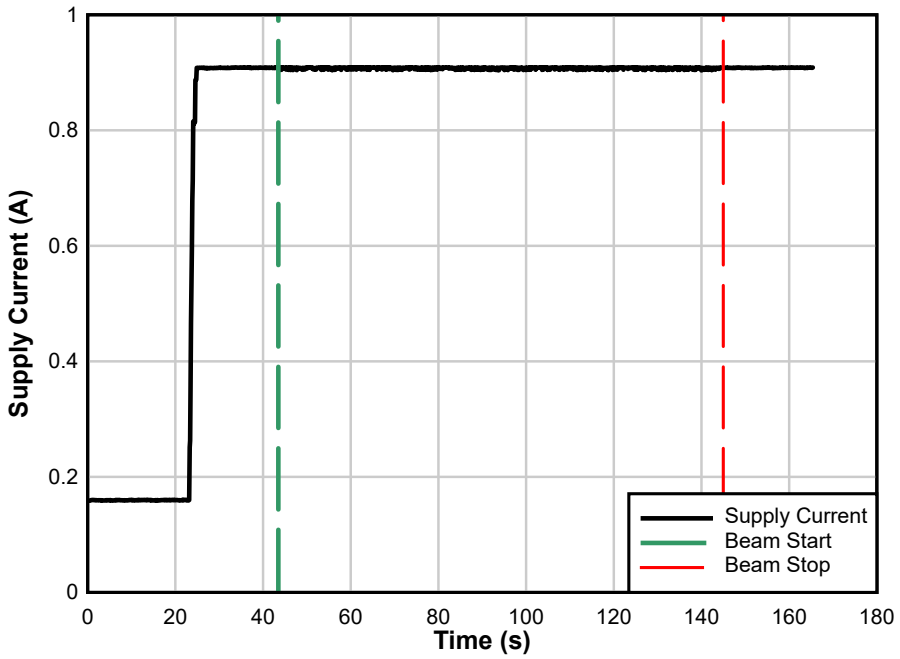

Figure 3-1. Supply Current for the ion run LET at 48 MeV-cm^2/mg and DUT Board Thermister Reading of 125°C

3.2 SEFI Results

SEFI was not detected during the ion run. During the ion run, the output of the DUT was momentarily upset, but the output always returned to the frequency programmed into the DUT. The DUT operated properly after the ion run and the registers did not need to be rewritten.

4 Summary

Under heavy ion testing, the LMK04832-SEP was found to be SEL and SEFI immune up to 48 MeV-cm^2/mg. SEL testing was performed at maximum operating voltage (3.45 V) and with the junction at greater than the maximum operating temperature (125°C). SEUs were seen but not captured or characterized.

5 References

1. Texas Instruments, *LMK04832-SEP Space Grade Ultra-Low-Noise JESD204B/C Dual-Loop Clock Jitter Cleaner* data sheet
2. Texas Instruments, *How Space-Enhanced Plastic devices address challenges in low-Earth orbit applications* E2E™ forum, Sree Alvarado, 2019
3. Texas Instruments, *JESD204B Overview* Texas Instruments High Speed Data Converter Training
4. Vendor Item Drawing V62/22612, Depart. of Defense, DLA Land and Maritime, Columbus OH, https://landandmaritimeapps.dla.mil/programs/Smcr/default.aspx
5. *Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices From Heavy Ion Irradiation*, EIA/JESD57
6. Texas Instruments, *LMK04832SEPEVM User's Guide*
7. "Cyclotron Institute, Texas A&M University," http://cyclotron.tamu.edu/ref

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