EVM User's Guide: LMKDB1102EVM, LMKDB1202EVM
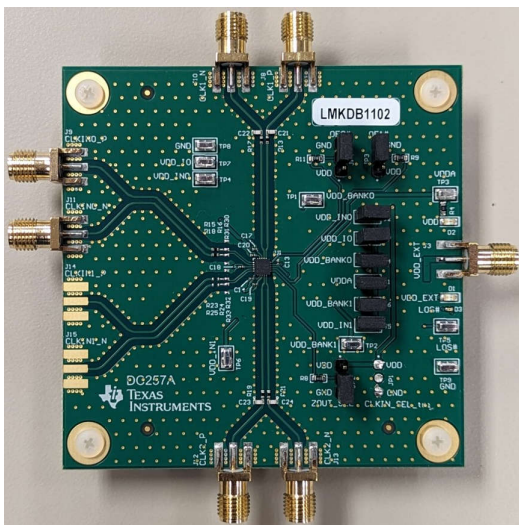# LMKDB1x02 Evaluation Module

Description

The LMKDB1102 and LMKDB1202 evaluation module (EVM) is designed to provide a quick setup to evaluate the LMKDB1x02 LP-HCSL buffer that supports PCIe Gen 1 to Gen 6. The printed circuit board (PCB) contains several jumpers to enable the LMKDB1x02 with desired user programming and setup. The evaluation module provides flexibility for compliance testing, system prototyping, and performance evaluation of the LMKDB1x02 device.
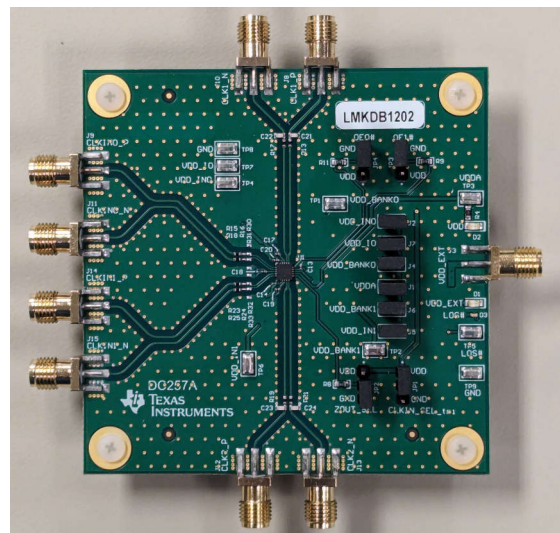
Features

- PCIe Gen 1 to Gen 6
- Setup via jumper headers and pins

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator

LMKDB1102EVM

LMKDB1202EVM

1 Evaluation Module Overview

1.1 Introduction

The LMKDB1102 and the LMKDB1202 use the same board layout. Pins 4 and 5 on the LMKDB1202 are CLKIN1_P and CLKIN1_N to support two inputs. The LMKDB1102 only has one input so these pins are left as no connect (NC). Because of this extra feature on the LMKDB1202, pin 7 is the CLKIN_SEL_tri pin for the LMKDB1202. This pin is a GND pin for the LMKDB1102. Input and outputs of LMKDB1x02 can be interfaced with external system for evaluating compatibility and performance through coaxial cable.

This user's guide contains information and support documentation for the LMKDB1x02 evaluation module (EVM). Included are the schematics, PCB layouts, and bill of materials for both the LMKDB1102EVM and LMKDB1202EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the LMKDB1x02EVM.

1.2 Kit Contents

LMKDB1x02EVM box contains:
- One LMKDB1x02EVM board (DC256A).

1.3 Specification

Some key specifications for LMKDB1x02 buffer and EVM are noted in Table 1-1.

Table 1-1. LMKDB1x02 Key Parameters

Parameter	Value
Ambient temperature	-40 to 105 ºC
Power supply	1.8V ± 10%, 3.3V ± 10%
Operating frequency	1MHz to 400MHz. (*automatic output disable* (AOD) disabled)
Output format	LP-HCSL

1.4 Device Information

The LMKDB1x02 is a high performance LP-HCSL buffer that supports PCIe Gen 1 to Gen 6. LMKDB1x02 has extremely low additive jitter, fail safe inputs, flexible power-up sequence, individual output enable pins, and loss of input signal (LOS) detection.

2 EVM Quick Start

Table 2-1 describes the default jumper configuration. Configure the EVM as specified in Table 2-1 for initial bring up.

Table 2-1. Default Jumper Configuration

Category	Reference Designator	Default Position	Description
Power	J1	1-2	Connects external supply to VDDA of device.
	J2	1-2	Connects external supply to VDD_IN0 of device.
	J5	1-2	Connects external supply to VDD_IN1 of device.
	J4	1-2	Connects external supply to VDD_BANK0 of device.
	J6	1-2	Connects external supply to VDD_BANK1 of device.
	J7	1-2	Connects external supply to IO pins on board (VDD_IO).
Output enable control pins	JP3 and JP4	2-3	Pull down to GND to enable output (OE#1 and OE#2).
Digital pins	JP2	2-3	ZOUT_SEL pulled low setting output impedance to 85Ω.
	JP1 (Not populated on the LMKDB1102)	2-3	CLKIN_SEL_tri pulled low to set CLKIN0 as the input source for all the outputs.

2.1 Setup

Figure 1-1 shows default jumper configuration for the EVM.

To begin using the LMKDB1x02EVM, follow the steps below.

1. Verify the EVM default jumper as described in Figure 1-1.
2. Connect a 3.3V external power supply to J3.
3. Connect 100MHz reference clock to CLKIN0_P/N. Refer to Table 3-6 for different input reference configurations.

2.2 EVM Measurements

Measurements can now be made on the clock outputs using an oscilloscope or a phase noise analyzer.

3 Hardware

3.1 EVM Configuration

The following sections describes power, logic, clock input, and output interfaces on the EVM and how to configure the EVM accordingly.

Some of the key components and the reference designator are noted in Table 3-1.

Table 3-1. Key Components Reference Designator and Descriptions

Item No.	Reference Designators	Description
1	U1	LMKDB1x02.
2	J3	External VDD through SMA port.
3	J9, J11, J14, and J15	SMA Ports for clock input (CLKIN#_P, CLKIN#_N). J14 and J15 are not populated on the LMKDB1102.
4	J8, J10, J12, and J13	SMA Ports for clock outputs (CLK#_P, CLK#_N).
5	JP2	ZOUT_SEL pin header jumper to select 85Ω or 100Ω output impedance.
6	JP1	CLKIN_SEL_tri pin header jumper to select which CLKIN drives which outputs. JP1 is not populated on the LMKDB1102.

3.1.1 Power Supply

The LMKDB1x02 has VDD, VDD_DIG, VDD_IN0, VDD_IN1, VDD_BANK0, and VDD_BANK1 supply pins that operate from 1.8V ± 10% and 3.3V ± 10% as shown on Section 5.1.

> **Note**
>
> **IMPORTANT:** The LMKDB1102 has different power supply pin names than the schematic. There was a change on the data sheet power supply pin names to remove confusion when completing drop-in replacements. Functionality remains the same on all power supply pins.

3.1.2 Logic Input and Outputs

The logic input and output pins on LMKDB1102 and LMKDB1202 provides option for output active / inactive control, loss of signal (LOS) detection, and output impedance selection. LMKDB1202 offers an additional input clock selection pin, CLKIN_SEL_tri.

Table 3-2. Clock Input Selection (only for LMKDB1202)

CLKIN_SEL_tri Input Level	Function
Low (default)	CLKIN0 is the input source for all outputs.
High	CLKIN1 is the input source for all outputs.
Hi-Z	CLKIN0 is the input source for OUT1 outputs and CLKIN1 is the input source for OUT2 outputs.

Table 3-3. Output Enable Pin Control

OE1# and OE2# Input Level	OUTPUT STATUS
Low (default)	Active
High	Inactive

Table 3-4. Loss of Signal (LOS) Detection (Status pin)

LOSb OUTPUT LEVEL	LOS STATUS
Low	Not detected
High	Detected

Table 3-5. LP-HCSL Differential CLock Output Impedance Select

ZOUT_SEL Input Level	Function
Low (default)	LMKDB1x02 has 85Ω output termination
High	LMKDB1x02 has 100Ω output termination

3.1.3 Clock Input

LMKDB1x02 can support different input interfaces for CLKIN# depending on the input swing and common mode voltage. There are four input interfaces type that can be configured on LMKDB1x02 using external components and internal termination schemes as shown in Figure 3-1. If using a signal generator and the LMKDB1102, then make sure to populate *R16* with a *100Ω* resistor or use internal / external 50Ω termination to ground. If using a signal generator, the LMKDB1202, and CLKIN1, also populate *R24* with a *100Ω* resistor or use internal / external 50Ω termination to ground.

1. DC Coupled HCSL / LP HCSL Input.
2. DC Coupled LVDS Input.
3. External AC Coupled Input.
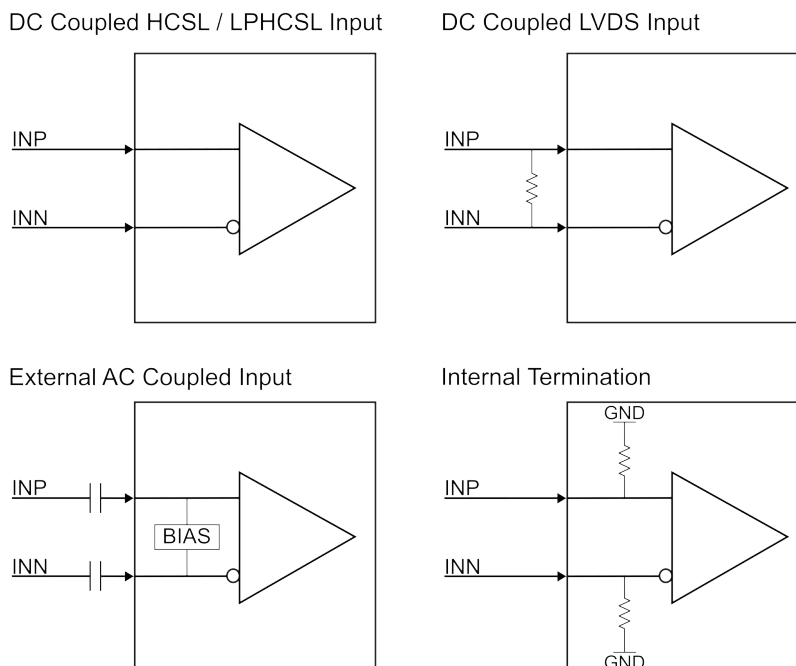4. Internal 50Ω to ground terminations.

Figure 3-1. Input Interfaces

Table 3-6 outlines how to setup all different interfaces supported by LMKDB1x02.

Table 3-6. Input Interfaces

Input Interface	Configuration
DC coupled HCSL / LPHCSL (default)	This is the default for the EVM for both clock inputs. *R15, R18* and/or *R23, R25* values are *0Ω* and *Input Interface Type* on *Input* page is selected to *DC Coupled* for each input being used. *R23* and *R25* are only required if using the CLKIN1 pins of the LMKDB1202.
DC coupled LVDS input	Populate *R16* and/or *R24* with a *100Ω* resistor and set *Input Interface Type* on *Input* page to *DC Coupled* for each DC coupled LVDS input. *R24* is only required if using the CLKIN1 pins of the LMKDB1202.
External AC coupled input	Replace *R15, R18* and/or *R23, R25* with *0.1uF* capacitor and set *Input Interface Type* on *Input* page to *AC Coupled* for each external AC coupled input. *R23* and *R25* are only required if using the CLKIN1 pins of the LMKDB1202
Internal termination	To enable internal 50Ω to ground terminations. Set the *Input Termination* on *Input* page to *Enabled*.

3.1.4 Clock Outputs

LMKDB1x02 has two differential clock outputs (CLK[1:2]_P/N). All the outputs are DC coupled with a capacitive load of 2pF.

> **WARNING**
> DC-coupled clocks must not be directly connected to RF equipment which cannot accept DC voltages greater than 0V, such as spectrum analyzers and phase noise analyzers.

3.1.5 Status Outputs, LEDs, and Test Points

LMKDB1x02EVM have status output signal from LMKDB1x02, LEDs, and test points to monitor signal and supply voltage on the board. Table 3-7 summarizes all the status signals and test points on the board.

Table 3-7. Status Output, LEDs, and Test Points

Function / Test Signal	Status Pin / LED Designator	Description
LOSb	TP5	Test point to monitor LOSb status.
	D1	LED status light for LOSb detection.
VDDA	D2	LED status light for VDDA supply pin.
	TP3	Test point for VDDA supply pins.
VDD_IN0	TP4	Test point for VDD_IN0 supply pins.
VDD_IN1	TP6	Test point for VDD_IN1 supply pins.
VDD_BANK0	TP1	Test point for VDD_BANK0 supply pins.
VDD_BANK1	TP2	Test point for VDD_BANK1 supply pins.
VDD_IO	TP7	Test point for VDD_IO supply pins.
VDD_EXT	D1	LED status light for VDD supply selected from USB option or External option through JP17.
GND	TP8, TP9	Test points for GND reference on the board.

4 Implementation Results

4.1 Typical Phase Noise Characteristic

Figure 4-1 shows a typical phase noise performance for 156.25MHz reference clock input from the SMA100B. Both the LMKDB1202 and the LMKDB1102 have the same performance.

LMKDB1x02EVM was configured in cascade mode to get these measurements, which were obtained by following these steps:

1. SMA100B → LMKDB1x02EVM input. Then, LMKDB1x02EVM to secondary LMKDB1x02 EVM. This was done to get a fast slew rate at the input. Other methods like clipping a circuit can be used to get a desired slew rate and square wave form as well outputted from the SMA100B.
2. Output phase noise is measured through a Balun to the differential waveform from the LMKDB1x02 into a single-ended waveform for the phase noise analyzer.
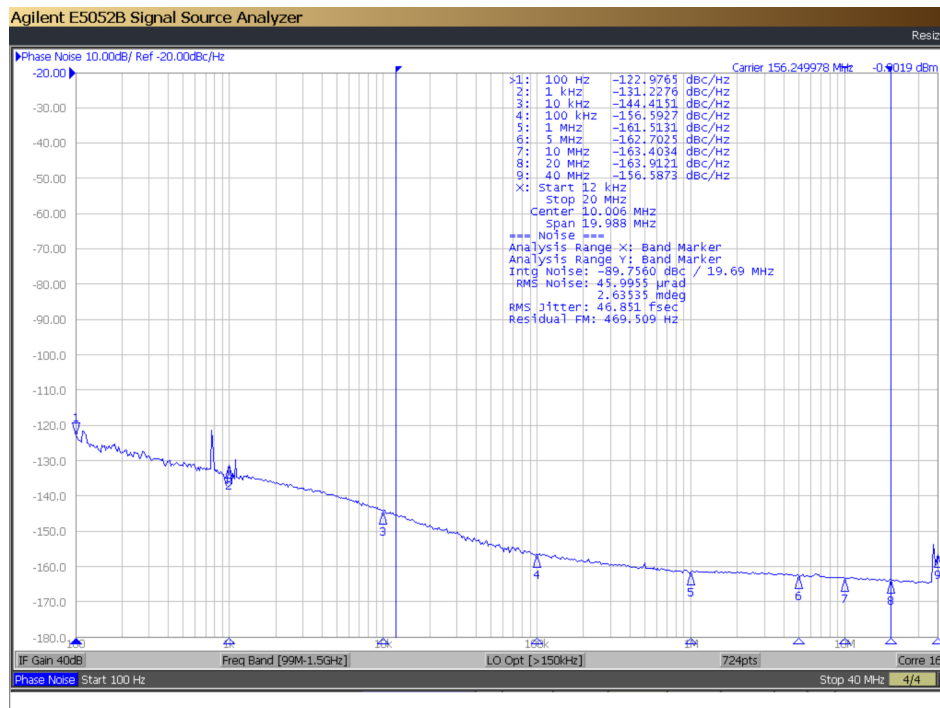

Figure 4-1. LMKDB1x02 Output Clock Phase Noise
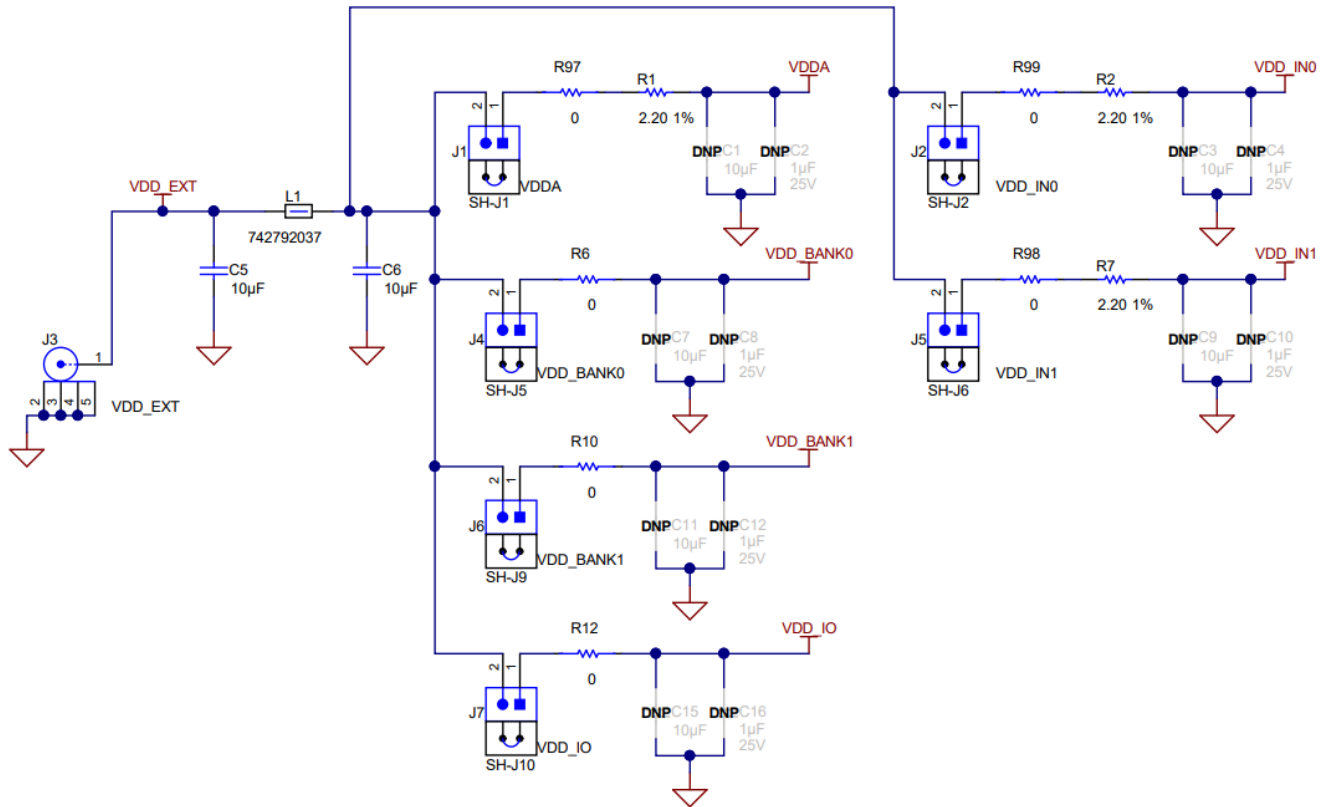
5 Hardware Design Files
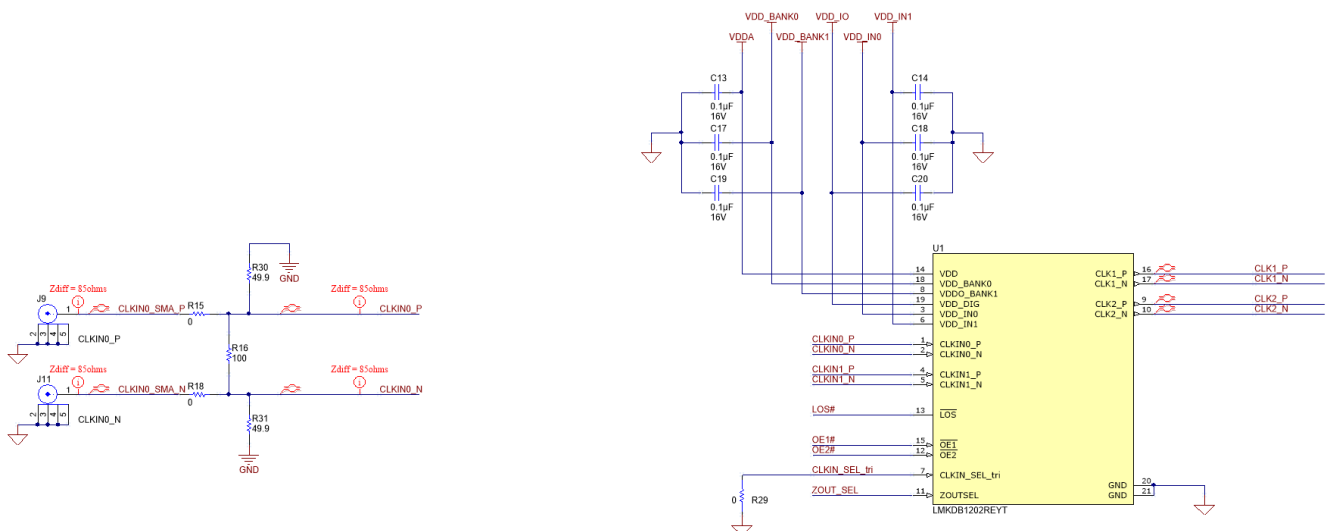
5.1 Schematics

Figure 5-1. Power Supply

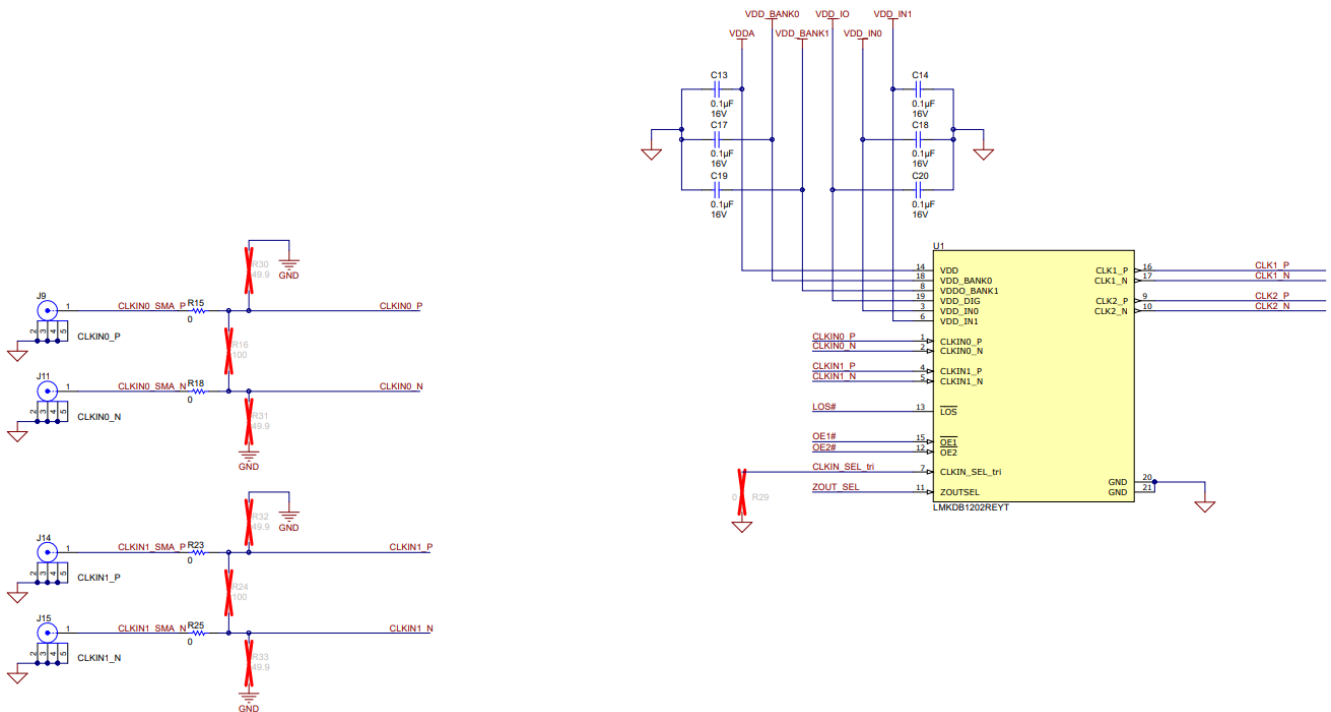**Figure 5-2. LMKDB1102 Device and CLKIN0_P/N Reference**

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Figure 5-3. LMKDB1202 Device and CLKIN#_P/N Reference
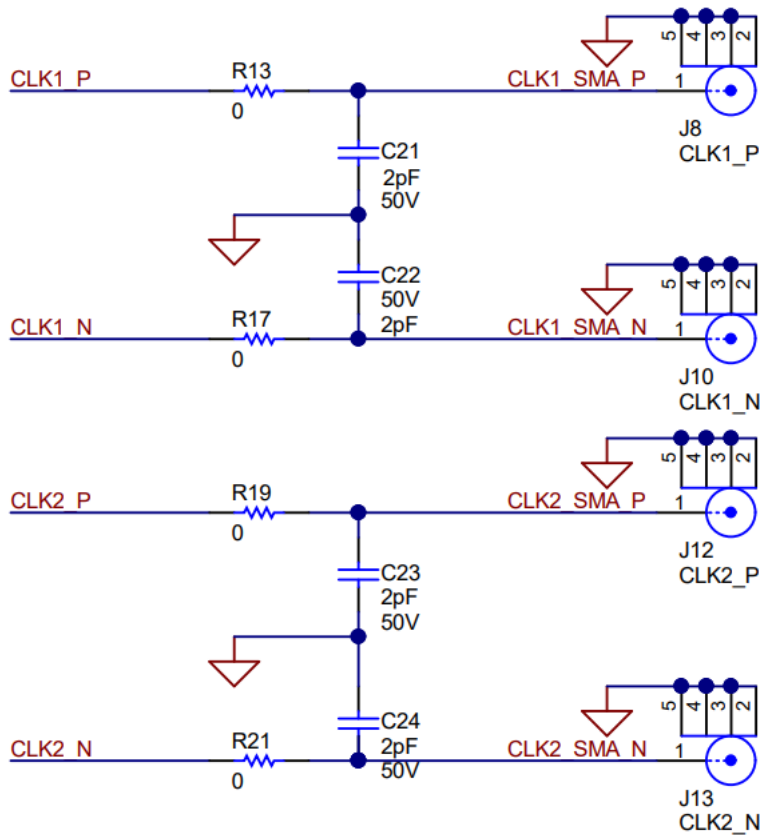
Figure 5-4. Clock Outputs CLK1 and CLK2

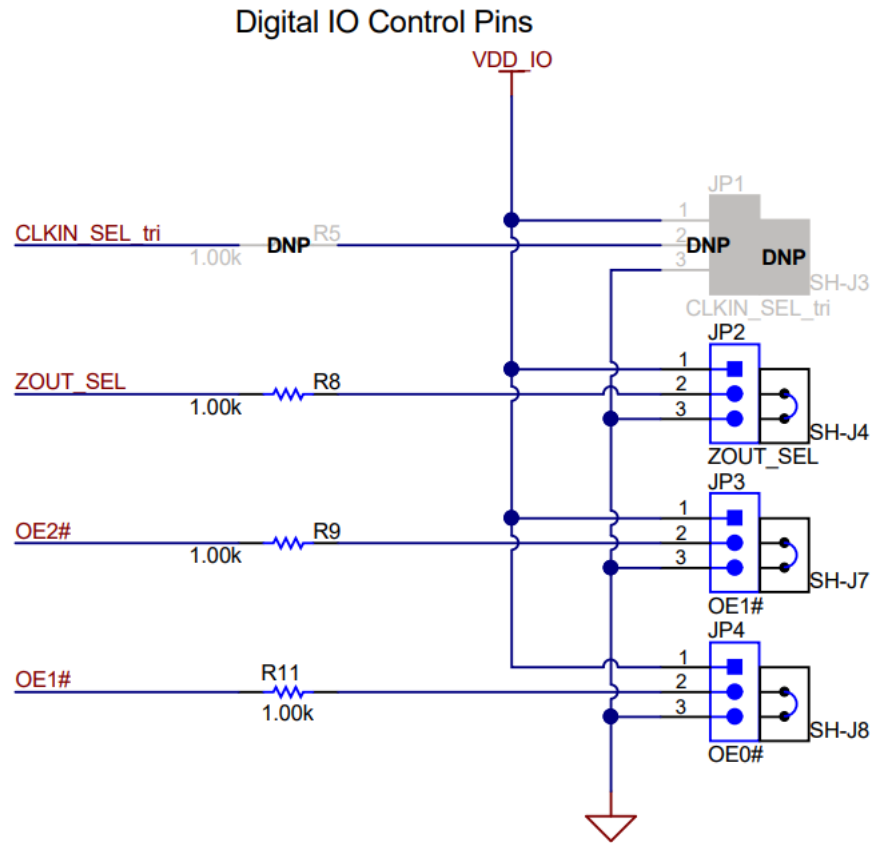## Digital IO Control Pins

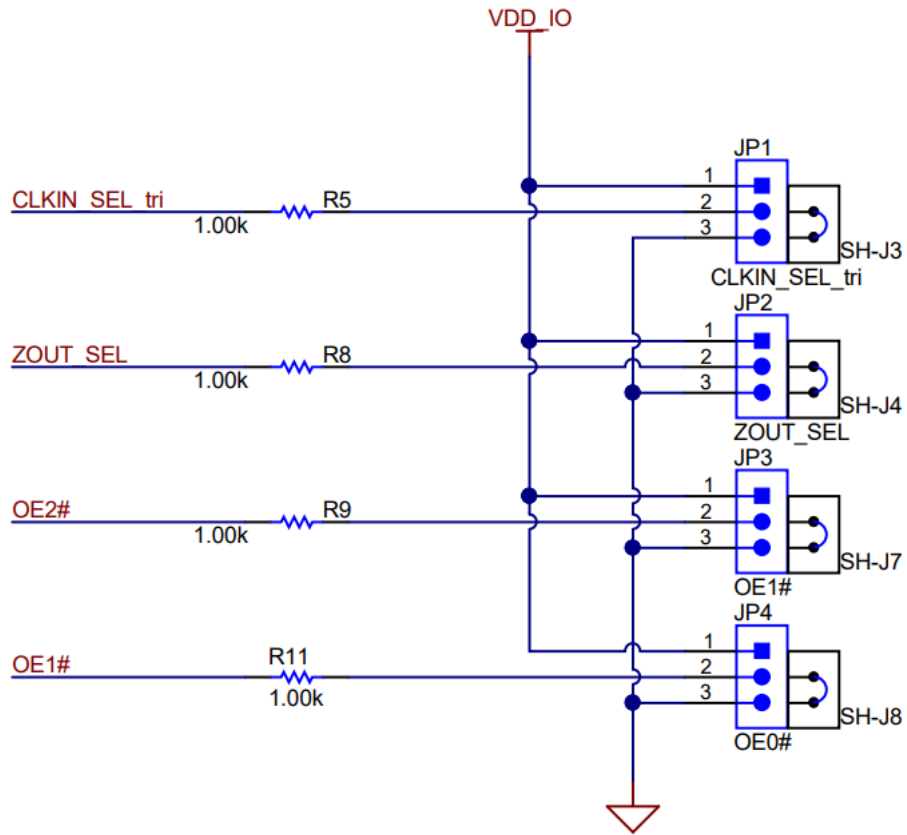**Figure 5-5. Output Enable Pins (OE#) and LMKDB1102 Logic I/O Jumpers**

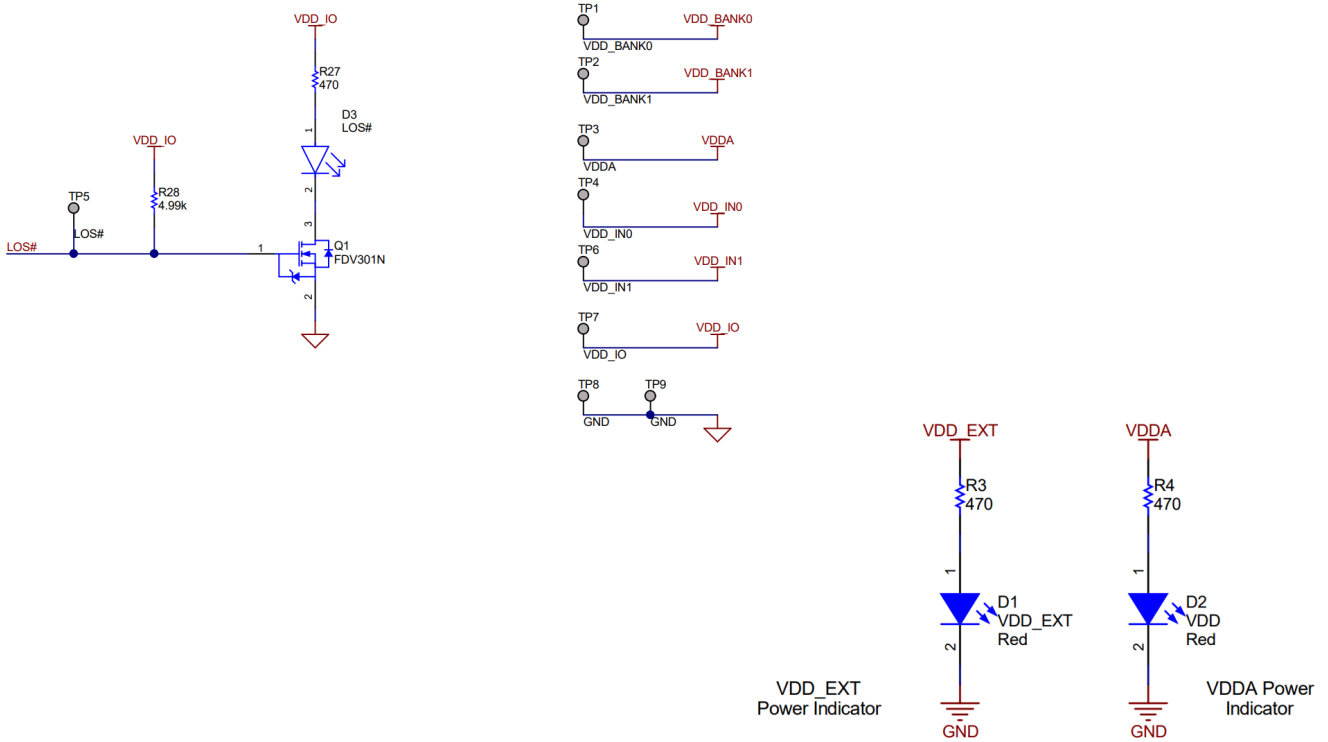**Figure 5-6. Output Enable Pins (OE#) and LMKDB1202 Logic I/O Jumpers**

Figure 5-7. Status LEDs and Test Points

5.2 PCB Layouts

Layer Stackup :

| Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	Top Layer	Copper	2.10mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	GND 1	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	10.00mil	4.2	
3	Signal-1	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	18.60mil	4.2	
4	PWR	Copper	1.40mil		
	Dielectric 4	FR-4 High Tg	10.00mil	4.2	
5	GND 2	Copper	1.40mil		
	Dielectric 5	FR-4 High Tg	6.00mil	4.2	
6	Bottom Layer	Copper	2.10mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

Figure 5-8. Layer Stackup
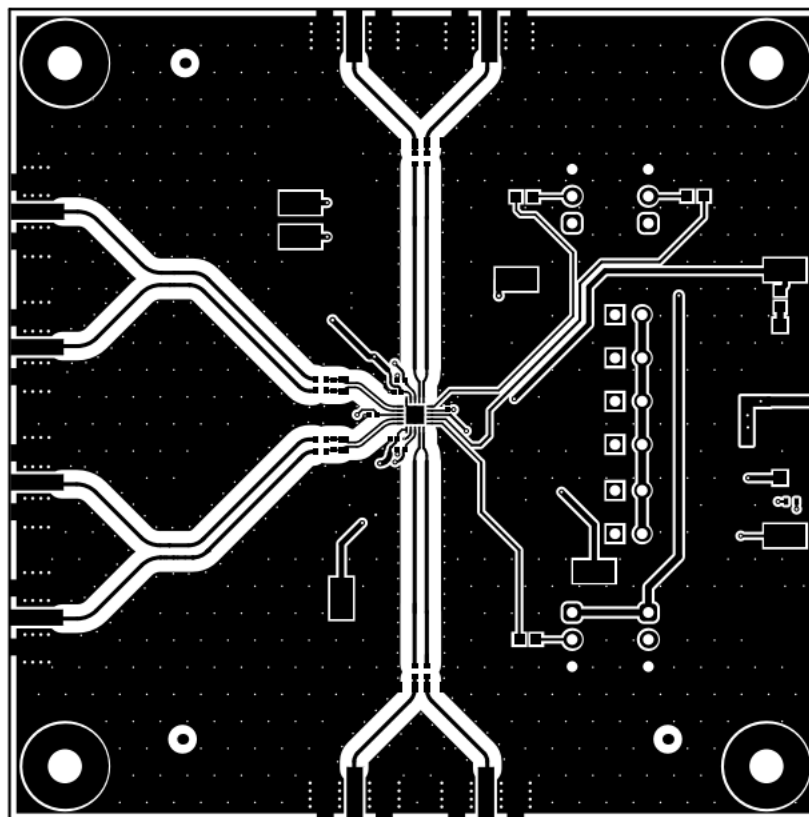
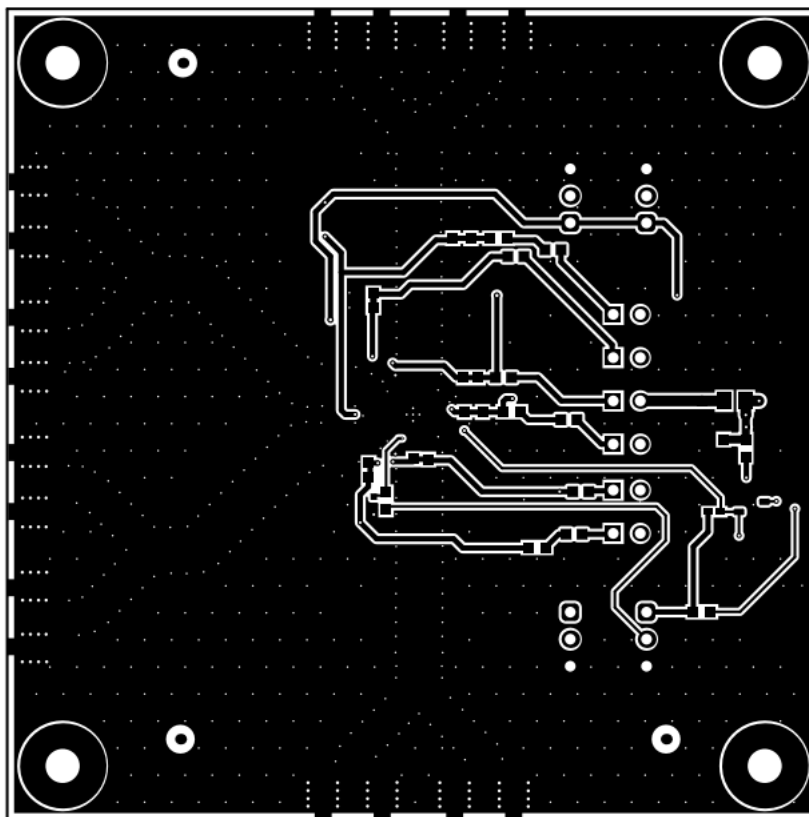**Figure 5-9. Top Layer (CLKIN / CLKOUT Signals)**
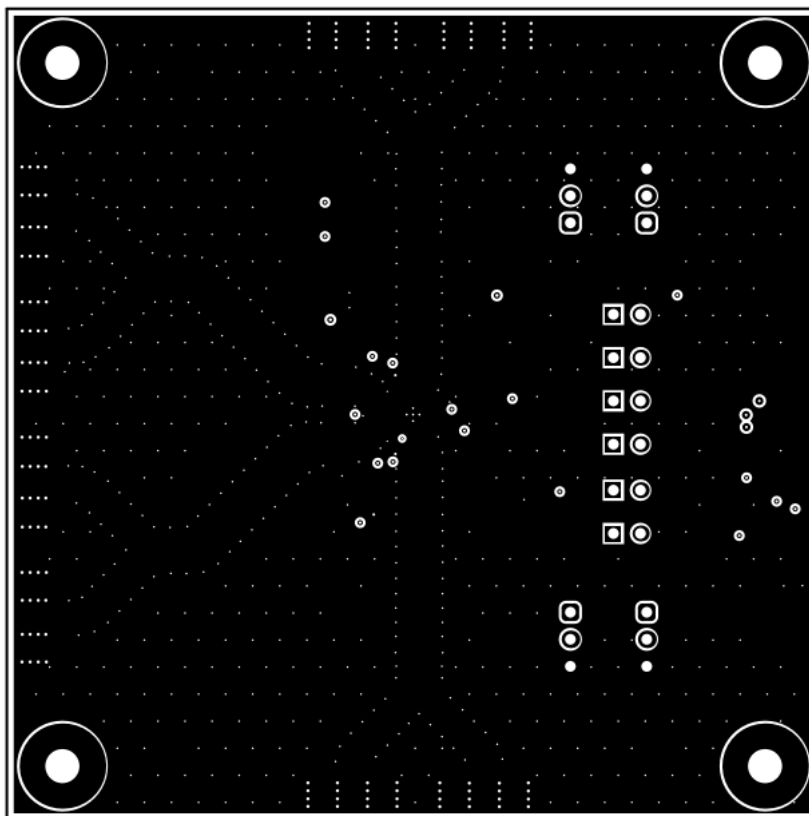
Figure 5-10. Bottom Layer
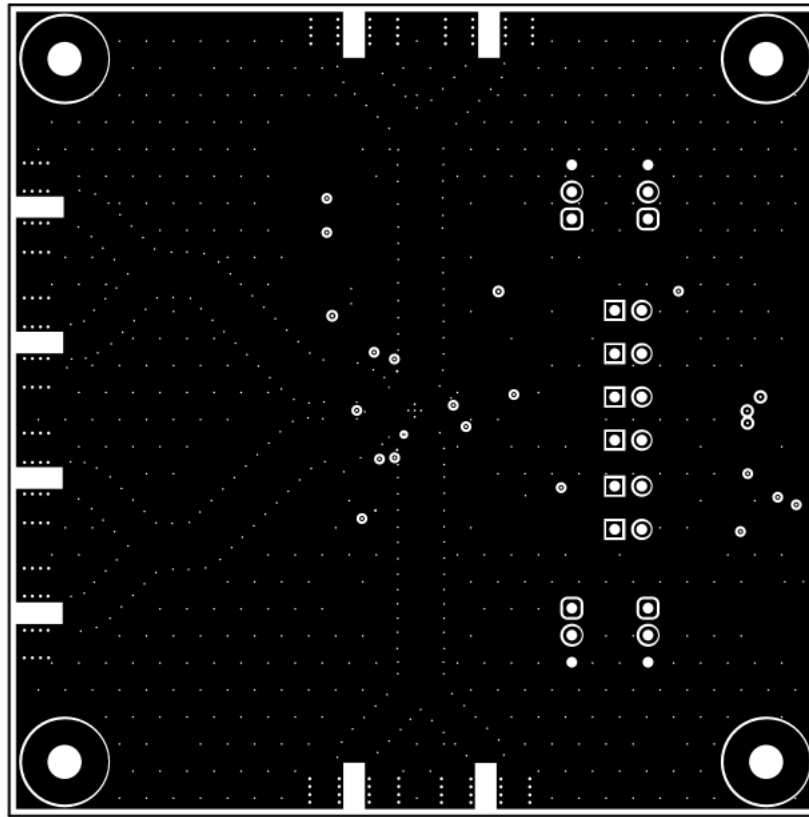

Figure 5-11. GND Layer 1

Figure 5-12. GND 2 Layer

5.3 LMKDB1102EVM Bill of Materials (BOM)

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC257	Any		
C5, C6	2	10uF	CAP, CERM, 10µF, 16V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata		
C13, C14, C17, C18, C19, C20	6	0.1uF	CAP, CERM, 0.1µF, 16V,+/- 10%, X7R, 0201	0201	0201BB104KW160	Passive Plus		
C21, C22, C23, C24	4	2pF	CAP, CERM, 2pF, 50V, +/- 12.5%, C0G/NP0, 0603	0603	C0603C209C5GACTU	Kemet		
D1, D2	2	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On		
D3	1		LED GREEN CLEAR 0402 SMD	0402	SM0402GC	Bivar		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J2, J4, J5, J6, J7	6		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity		
J3, J8, J9, J10, J11, J12, J13	7		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.		
JP2, JP3, JP4	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
L1	1	330 ohm	Ferrite Bead, 330 ohm at 100MHz, 2A, 0805	0805	742792037	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
Q1	1	25V	MOSFET, N-CH, 25V, 0.22A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor	None	
R1, R2, R7	3	2.20	RES, 2.20, 1%, 0.1 W, 0603	0603	ERJ-3RQF2R2V	Panasonic		
R3, R4, R27	3	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale		
R6, R10, R12, R97, R98, R99	6	0	0 Ohms Jumper Chip Resistor 0603 (1608 Metric) Metal Element	0603	WSL060300000ZEA9	Vishay		
R8, R9, R11	3	1.00k	RES, 1.00 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE071KL	Yageo America		
R13, R15, R17, R18, R19, R21	6	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R28	1	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America		
R29	1	0	RES Thick Film, 0Ω, 0.2W, 0402	0402	CRCW04020000Z0EDHP	Vishay Dale		

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH-J1, SH-J2, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10	9	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone		
U1	1		PCIe Gen 1 to Gen 6 Ultra Low Jitter, 2:2 LP-HCSL Clock Buffer and Clock MUX	WQFN20	LMKDB1102REYT	Texas Instruments		

5.4 LMKDB1202EVM Bill of Materials (BOM)

Table 5-2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC257	Any		
C5, C6	2	10uF	CAP, CERM, 10µF, 16V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata		
C13, C14, C17, C18, C19, C20	6	0.1uF	CAP, CERM, 0.1µF, 16V,+/- 10%, X7R, 0201	0201	0201BB104KW160	Passive Plus		
C21, C22, C23, C24	4	2pF	CAP, CERM, 2pF, 50V, +/- 12.5%, C0G/NP0, 0603	0603	C0603C209C5GACTU	Kemet		
D1, D2	2	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On		
D3	1		LED GREEN CLEAR 0402 SMD	0402	SM0402GC	Bivar		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J2, J4, J5, J6, J7	6		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity		
J3, J8, J9, J10, J11, J12, J13, J14, J15	9		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.		
JP1, JP2, JP3, JP4	4		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
L1	1	330 ohm	Ferrite Bead, 330 ohm at 100MHz, 2A, 0805	0805	742792037	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
Q1	1	25V	MOSFET, N-CH, 25V, 0.22A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor		None
R1, R2, R7	3	2.20	RES, 2.20, 1%, 0.1 W, 0603	0603	ERJ-3RQF2R2V	Panasonic		
R3, R4, R27	3	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale		
R5, R8, R9, R11	4	1.00k	RES, 1.00 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE071KL	Yageo America		
R6, R10, R12, R97, R98, R99	6	0	0 Ohms Jumper Chip Resistor 0603 (1608 Metric) Metal Element	0603	WSL060300000ZEA9	Vishay		
R13, R15, R17, R18, R19, R21, R23, R25	8	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R28	1	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America		

Table 5-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10	10	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone		
U1	1		PCIe Gen 1 to Gen 6 Ultra Low Jitter, 2:2 LP-HCSL Clock Buffer and Clock MUX	WQFN20	LMKDB1202REYT	Texas Instruments		

6 Compliance Information

6.1 Compliance and Certifications

Refer to *LMKDB1102EVM Declaration of Conformity (DoC)* (SSZQSB4) and *LMKDB1202EVM Declaration of Conformity (DoC)* (SSZQSB5)

7 Additional Information

7.1 Trademarks

All trademarks are the property of their respective owners.

8 References

For additional information on LMKDB1x02, refer to *LMKDB1120/1108/1104/1102/1204/1202 PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX*.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

    1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

    1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

    2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

    2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

    2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:
EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの

措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4   *EVM Use Restrictions and Warnings:*

4.1   EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2   User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3   *Safety-Related Warnings and Restrictions:*

4.3.1   User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2   EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4   User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5.   *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6.   *Disclaimers:*

6.1   EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2   EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7.   *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.