Technical White Paper

How and Why to Use Single Twisted-Pair Ethernet (SPE) for Industrial Robotics Environments

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ABSTRACT

Communication in robotics system designs is undergoing a transformation as it keeps pace with the fourth industrial revolution, or industry 4.0. In the status quo, robot communications must be robust, accurate, have excellent timing characteristics and neither hinder axis movement, nor be negatively impacted by it. Several important, but disparate, communication interfaces have evolved to meet the stringent requirements of robotics communications and have done so for many years. Increasing speed and bandwidth requirements from robots is starting to exceed the capabilities of these very effective interfaces.

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1 Introduction

As designers look for new ways to meet faster cycle time and higher throughput to meet big data requirements, and have these wider-bandwidth systems work at the highest efficiencies with minimal downtime, designers can also wish to minimize impact on the upgrade by reusing existing cabling infrastructure. Most also employ advanced features like smarter diagnostics, higher safety specifications and faster and better real-time characteristics for motor control.

Robotic system architectures must meet communication interface requirements like bandwidth margin. As bandwidth requirements continue to increase, designers are incorporating both Ethernet and optical designs that are faster than legacy interfaces like RS-485 and Controller Area Network (CAN). However, when moving to Ethernet, consider how to minimize latency in the real-time performance of the Ethernet protocol, either through industrial Ethernet protocols such as Ethernet/IP, EtherCAT, Profinet, and so forth, or by implementing a proprietary communication protocol.

This article discusses the benefits of SPE (Base-T1) for robotics applications as well as key challenges when designing with compact, efficient, robust and low-noise communication interfaces for robotic systems. These challenges need to be understood to implement single twisted-pair Ethernet in the robot systems and still achieve the needed performance to operate the robot efficiently.

Typically, two key design parameters are data rate and cable size or length. These two parameters are related which means that the cable length for some communication interfaces define the data rate which can be achieved. A second parameter is the physical amount of cables and connector pins which are needed to implement the interface.

Table 1-1 lists the standard data rates and cable lengths of PHY types typically used in robotic systems.

Table 1-1. Physical Communication Interface Features

Communication Interface	Data Rate	Cable Length	Twisted-Pair Wires
4mA to 20mA I/O	0.01Mbps(1)	3000m	1
HART	00012Mbps	3000m	1
CAN	1Mbps	40m	1
CAN-Flexible Data Rate (FD) or CAN-Signal Improvement Capability	10Mbps	10m	1
RS-485	20Mbps	40m	1
100Base-TX	100Mbps	100m	2
1000Base-TX	1,000Mbps	100m	4
1000Base-SX	1,000Mbps	1,000m	Multimode fiber
1000Base-LX	1,000Mbps	5,000m	Single-mode fiber
Low-voltage differential signaling	360Mbps	10m	1
100Base-T1	100Mbps	50m (UTP) 100m (STP)	1
1000Base-T1	1,000Mbps	15m (UTP) 40m (STP)	1
10Base-T1L	10Mbps		1
10Base-T1S	10Mbps		1

(1) It is not usual to define the 4mA to 10mA I/O within the quantity bps as this is a one-bit signal with a predefined frequency, however it is provided here for data speed comparison.

When considering the data rate and cable lengths required for a particular robotic system, also consider the cable aging (highly affected by the movement of the robot), cost, diameter, and weight of the cables used in the system. The cable tree of the manipulator In a robotic arm is typically replaced every 2 to 3 years due to cable aging. This is performed as preventive maintenance, without testing the cable function. With this in mind, by reducing the number of wires (which can age) and by introducing smart diagnostic features in the PHY (to understand the ongoing quality of the cable), there are fewer points of failure and cable and connector health indicate a need to change cabling, rather than arbitrarily doing so every couple of years, needed or not. Another benefit is that the mechanical construction of the arm gets smaller and more cost effective due to less space being needed to route smaller cables.

There are specifications beyond data rate and cable selection which impact the performance of a robotic system and so these specifications must be understood. The following list shows some system elements which influence the system performance of robots and these points must be considered in the design of a system.

- Deterministic real-time communication with minimum latency
- Jitter between different packets
- Electromagnetic compatibility of the Base-T1 interface
- Hardware and software factors to achieve bandwidth and latency
- Diagnostics for detecting cable defects

2 System Challenges to Understand When Changing Communication Interface

Complex systems like robots have several communication interfaces – and potentially a mix of different interfaces – to support because of different subsystem requirements. Figure 2-1 shows a decentralized robot system with several communication interface paths, each of which has a different specification.

Changing to SPE from these interfaces provides benefits for the overall system cost and mechanical dimensioning. However, SPE also creates the need to make sure that the necessary timing performance is possible.

The green lines in Figure 2-1 show the communication interface, which usually employs a real-time protocol that makes sure deterministic communication with a high data rate for amount of data transferred. The blue lines show the motor drive encoder interface, which is typically accomplished with either a proprietary digital protocol based on RS-485, or an analog encoder interface.

The internal communication path of a robot operates in proximity to the location of switching phases of the motors. This implementation can reduce the number of cables and power levels in the robot, while also eliminating the need for cooling at the robot joint. However, moving the placement of power electronics into the manipulator has the potential to cause continuous noise in the communication interface of the system. This in turn creates a new challenge of losing communicated data due to the poor noise performance of the chosen interface or design. In SPE, performance in noisy environments is highly dependent on the type of PHY decoupling selected. Section 4 explains galvanic and capacitive decoupling. As previously described, another challenge is that the manipulator is constantly moving the cable around, damaging the cable over time.

Battery-driven robots also benefit from reducing the number of cables with SPE, since doing so reduces weight, increases system efficiency and so maximizes time between charges (extends battery life).

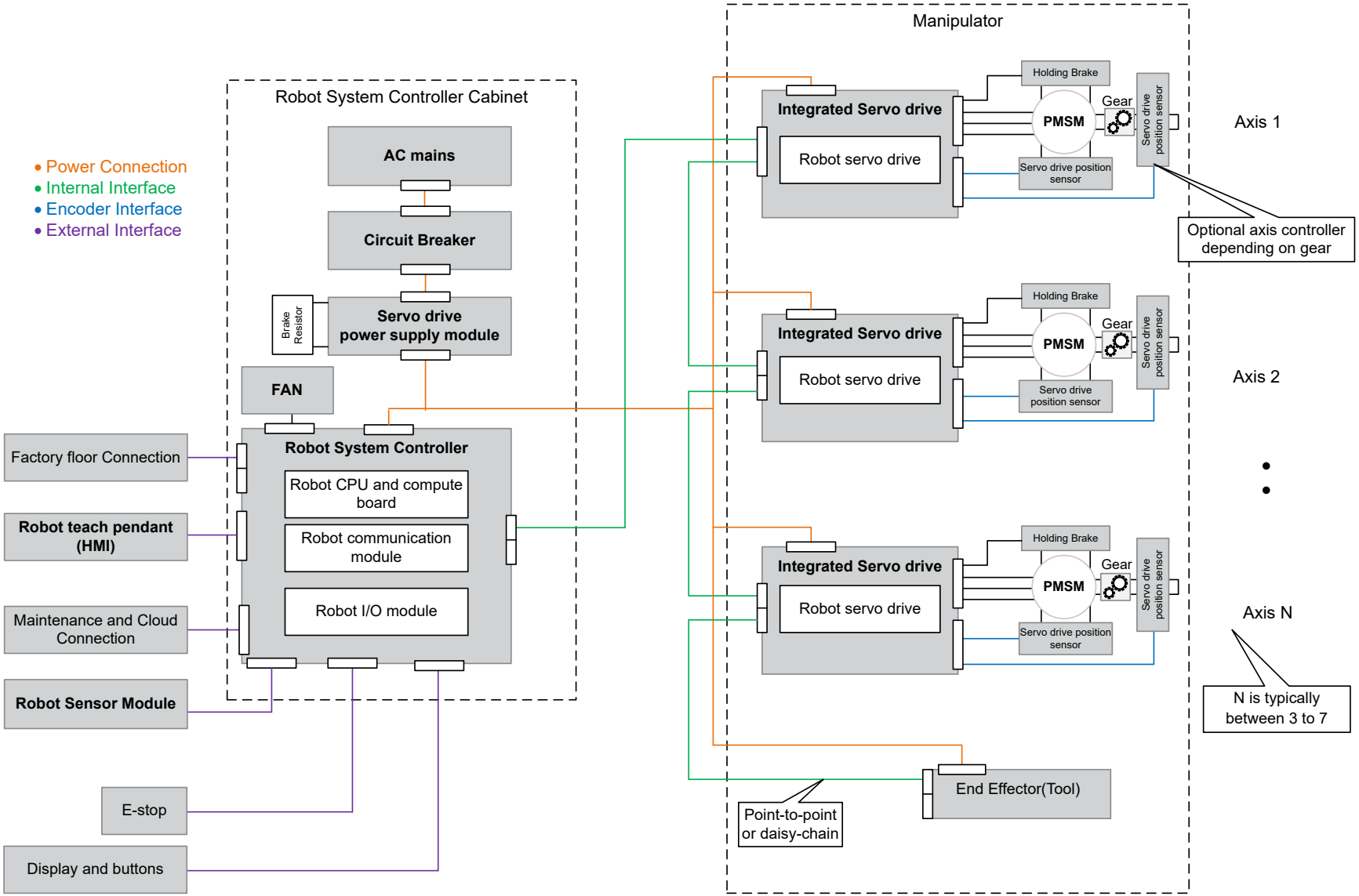

Figure 2-1. Decentralized Robot Architecture Example

3 Deterministic Real-Time Communication With Minimum Latency

Figure 3-1 shows latency and jitter affecting the real-time performance of a robotic system, which requires quantifying to make sure the necessary performance timings are possible.

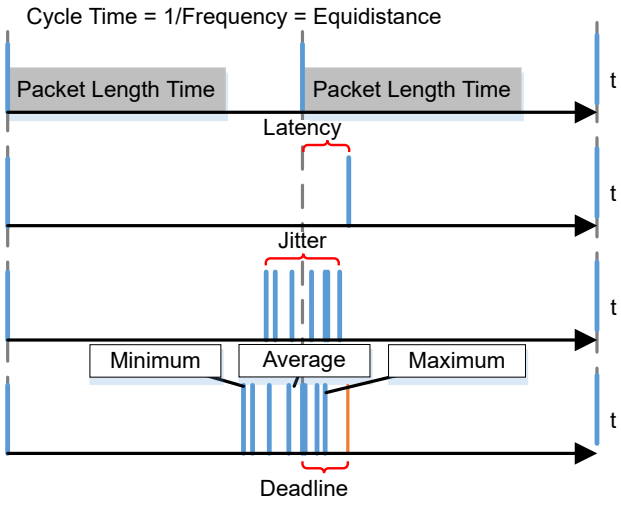

Figure 3-1. Key Points of Understanding Determinism

Quantifying jitter and latency performance define the maximum acceleration and speed at which the robot has controlled movements. Tests must be conducted on each physical layer (PHY) to determine the jitter and latency performance. The results of these tests provide understanding of the timing effects that a potential change of interface can have on system performance.

Therefore, the designer must be aware of the deadline requirement of the protocol, with this defined it can easily be determined if the chosen PHY can support the needed requirement by measuring the jitter and latency of this interface.

The quantification of determinism of the physical layer also influences the industrial protocol chosen. To date, no common industrial protocol has been finalized for use over a SPE PHY layer. Instead, designers have to either develop proprietary systems, or use protocols that have not been standardized, adding time and risk to development of a product. There are ongoing efforts to address this obstacle to adopting SPE in industrial environments, and there are already systems in the market using the technology.

To quantify and asses the deterministic performance of the Single Twisted Pair PHY, a test setup was built to perform these measurements. The test was built to emulate a daisy-chained industrial system, where test points were added to ease the measurements of the TX_CTRL and RX_CTRL MII signals. Figure 3-2 shows the system test setup.

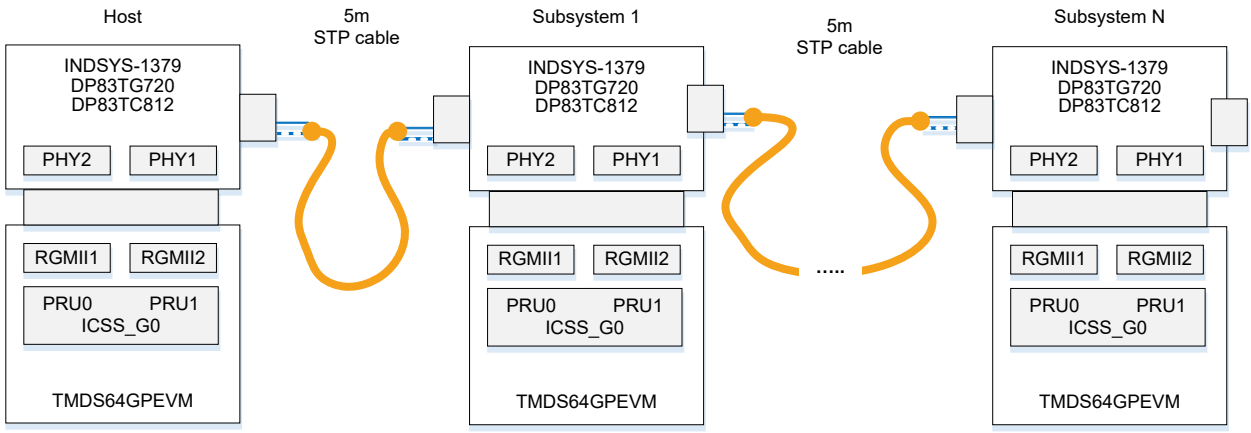

Figure 3-2. System Test Setup for STE Latency Measurement

The host transmits and defines the Ethernet packet which is sent onto the cable. Subsystem 1 is built as a repeater function which forwards the packet to the next board. Subsystem N is built as a loop-back function which receives the Ethernet packet and transmits the packet back onto the same cable.

The modules are needed to emulate an industrial daisy-chained system which is typically used in industrial protocols like EtherCAT, Simple Open Real-Time Ethernet (SORTE), Profinet, and so forth.

Each of the modules has two Ethernet PHYs (PHY1 and PHY2) which add some latency to the transfer of the data packet. Figure 3-3 illustrates contributors of this latency.

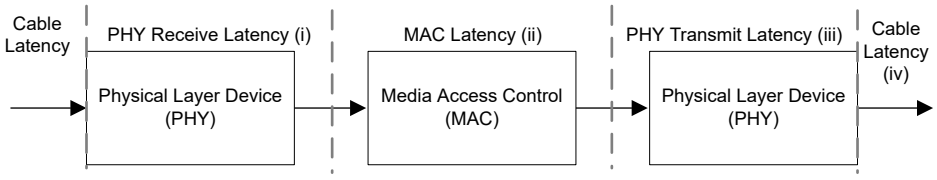

Figure 3-3. Contributors of Latency in the Communication Layers

Figure 3-3 shows how these PHYs and the MAC contribute to latency. Each contributor is consecutively numbered from (i) to (iii). Figure 3-4 illustrates how to relate these numbered latencies back to the subsystems in Figure 3-2.

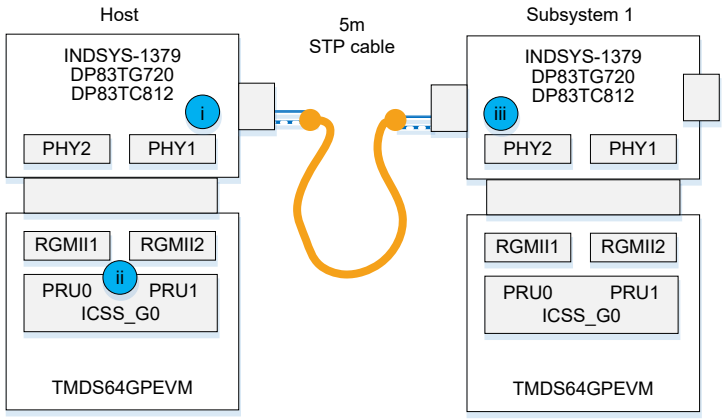

Figure 3-4. Latency Contributors in Each Subsystem

The latency contribution in Figure 3-4 is shown in one direction, for the measurement this means that for the host sending a data packet to subsystem 1, this packet is now in the MAC sent back from subsystem 1 to the host. This setup makes it possible to measure the cycle times of TI's 100BASE-T1 and 1000BASE-T1 PHYs on a system level. In this case as previously stated, a 0.5m STP cable was used during testing.

The following conditions apply for the screen grabs shown in Figure 3-5 through Figure 3-7.

- Measurement point 1 shows the total delay contribution of PHY1 (i) and PHY 2 (iii) showing the combined RX and TX latency of PHY.
- Measurement point 2 shows the delay contribution of MAC layer of the system.
- Measurement point 3 shows the total delay contribution of PHY2 (i) and PHY 1 (iii) showing the combined RX and TX latency of PHY.

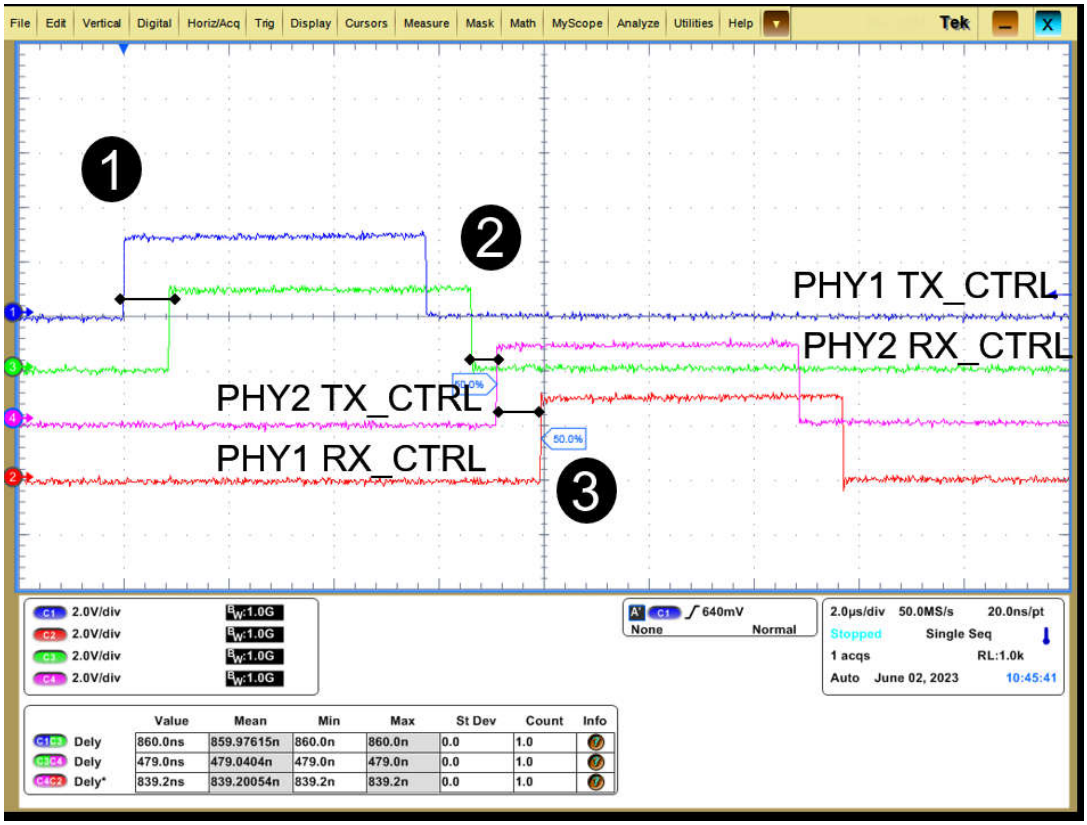

Figure 3-5. DP83TC812 - 100BASE-T1 Cycle and Latency Timings

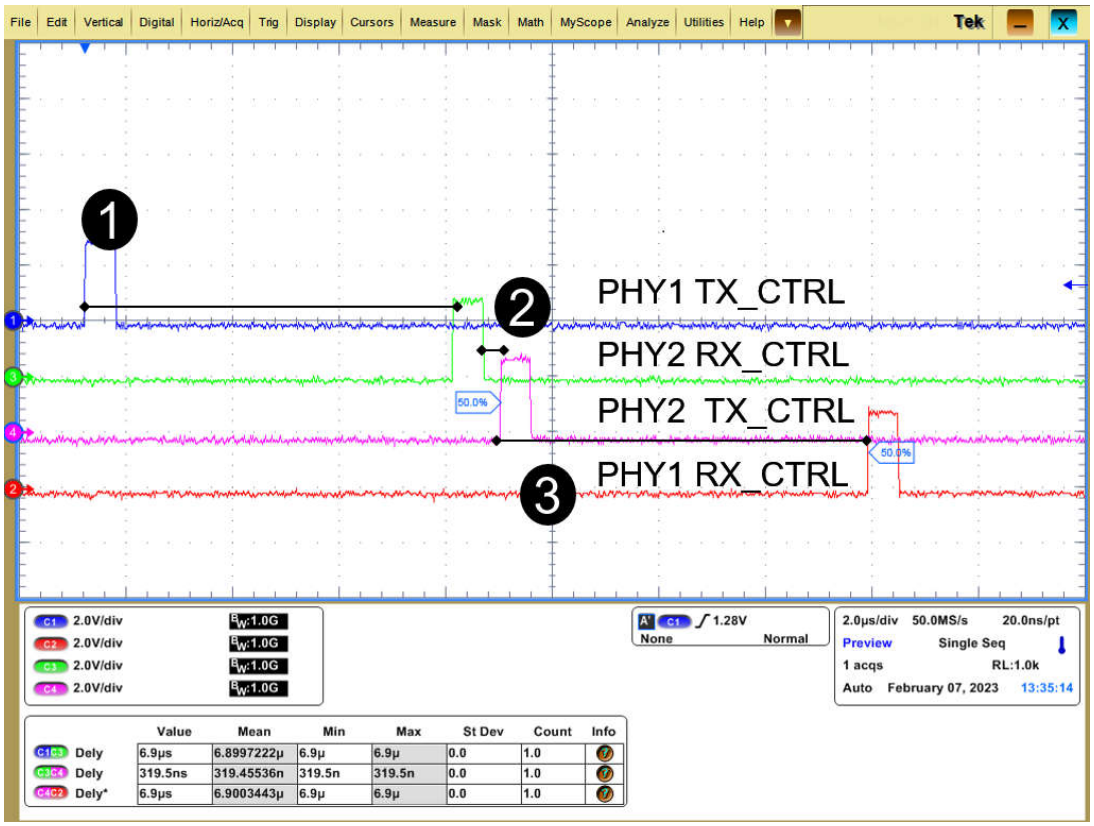

Figure 3-6. DP83TG720 - 1000BASE-T1 Cycle and Latency Timings, RS Encoder Block Enabled

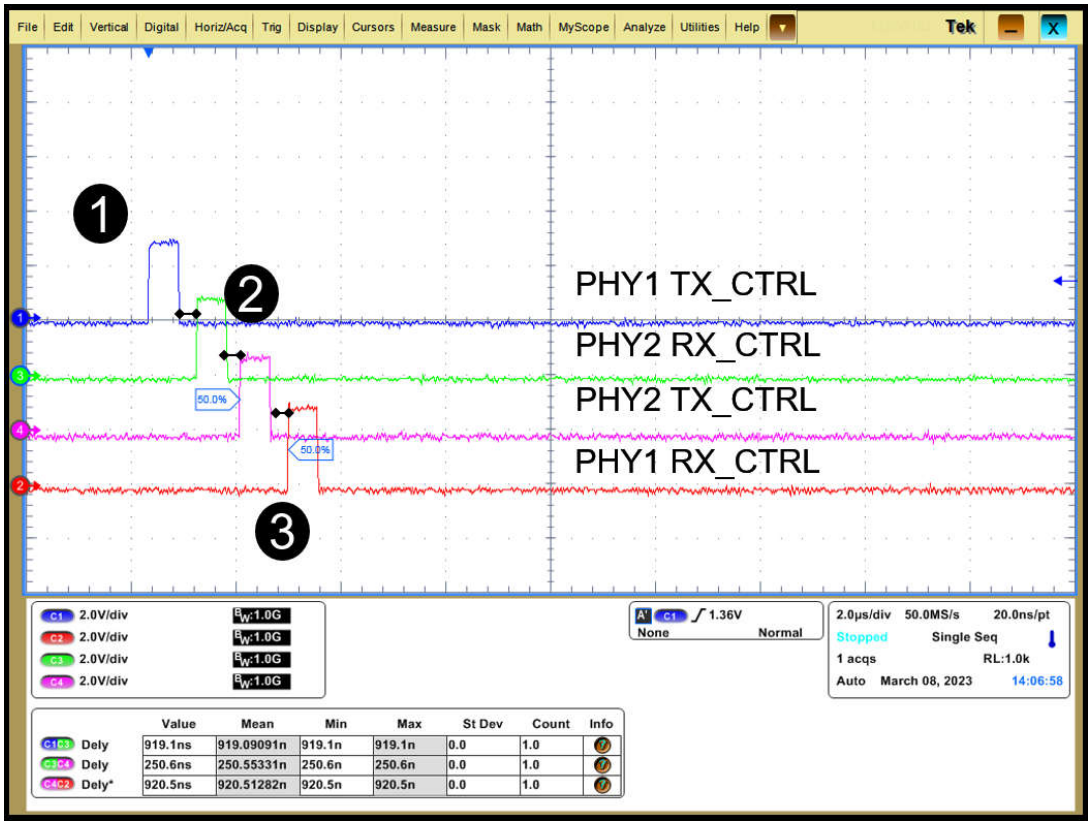

Figure 3-7. DP83TG720 - 1000BASE-T1 Cycle and Latency Timings, PHY RS Encoder Block Disabled

Figure 3-5 shows the RGMII latency of the DP83TC812 PHY and the MAC latency of the AM64x Sitara™ processor. The PHY latency specification is also in the *DP83TC812x-Q1 TC-10 Compliant 100BASE-T1 Automotive Ethernet PHY* data sheet. Figure 3-6 similarly shows the RGMII latency of the DP83TG720 PHY and the MAC latency of the AM64x Sitara processor.

Cycle time is also affected by packet length, which is also needed to understand the bandwidth required on the chosen PHY layer. For the test setup, an Ethernet packet was defined the following way: 64 bytes of payload and 12 bytes of payload overhead. On top of the delay from system latency, the packet length time also needs to be considered. Table 3-1 lists the measured values from testing the system indicated in Figure 3-4.

By default, the DP83TG720 implements a Reed Solomon (RS) encoder for error control coding (ECC) and forward error correction (FEC). This encoding adds non-trivial latency to cycle time. For more information on Reed Solomon encoding, see the *Reed Solomon Decoder: TMS320C64x Implementation* application note.

Table 3-1. System Performance if 100Base-T1 PHY Including 5m Cable, Assuming Same MAC Latency for RX and TX Times

Ethernet Type	PHY Latency (1) (3) Transmit and Receive	MAC Latency (2)	Total Latency	Packet Length Time (76 Bytes)	Packet Length and Latency
RGMII – 100Base-T1	860ns	480ns	1340ns	5666ns	7006ns
RGMII – 1000Base-T1, RS FEC bypass mode disabled	6900ns	320ns	7430ns	566ns	7996ns
RGMII – 1000Base-T1, RS FEC bypass mode enabled	920ns	250ns	1450ns	566ns	2016ns

What does this mean for system performance for a robot arm with 7 to 10 subsystems on a daisy-chain communication branch? The data in Table 3-2 is taken under the assumption that the packet is completely received before it is retransmitted. This comparison assumes that the full packet is sent as a half-duplex data transfer, even though the Base-T1 can support full duplex. Using the full duplex capability of the transceiver can improve the latency of the data transfer; however, using this feature of the PHY is heavily dependent upon the protocol used to implement the system.

The results in Table 3-2 indicate the time contributions from PHY latency, MAC latency, and packet length time

Table 3-2. Half Duplex Cycle Time Through 10 Subsystems

Ethernet Type	Host	Subsystem 1	Subsystem 2	Subsystem 3
RGMII – 100Base-T1	0	7.006µs	14.012µs	21.018µs
RGMII – 1000Base-T1, Encoder Enabled	0	7.946µs	15.892µs	23.838µs
RGMII – 1000Base-T1, Encoder Disabled	0	2.016µs	4.032µs	6.048µs
	Subsystem 4	**Subsystem 5**	**Subsystem 6**	**Subsystem 7**
RGMII – 100Base-T1	28.024µs	35.030µs	42.036µs	49.042µs
RGMII – 1000Base-T1, Encoder Enabled	31.784µs	39.730µs	47.676µs	55.622µs
RGMII – 1000Base-T1, Encoder Disabled	8.064µs	10.08µs	12.096µs	14.112µs
	Subsystem 8	**Subsystem 9**	**Subsystem 10**	Full Loopback
RGMII – 100Base-T1	56.048µs	63.054µs	70.060µs	140.12µs
RGMII – 1000Base-T1, Encoder Enabled	63.658µs	71.514µs	79.460µs	158.92µs
RGMII – 1000Base-T1, Encoder Disabled	16.128µs	18.144µs	20.16µs	40.32µs

This example only takes into account the time required to move the packet from the host to subsystem 10, the latency value is defined using MAC delay plus RX (PHY1) and TX (PHY2) latency to account for sending a packet through all subsystems and back to the host, the time is doubled, showed in the *Full Loopback* column in Table 3-2.

For this robot system, sending a packet back and forth can be performed every 40.32µs at the fastest, to 158.92µs at the slowest using 10 daisy-chained subsystems. These times limit the range of what is possible to achieve for a system-level defined maximum communication time.

For a robot using up to 10 subsystems, this time interval is typically fast enough to achieve good system performance.

4 Electromagnetic Compatibility of the Base-T1 Interface

Several standards help make sure that continuous noise does not cause the system to fail; one example is the International Electrotechnical Commission (IEC) 61000-4 tests for radiated and conducted noise types. The standard's accepted criterion level shows how well the system can perform when the system is subjected to noise. The IEC 61000-4-4 electrical fast transient (EFT) test, in particular, is a compliance test that simulates the switching phases of a motor.

To pass the EFT test, optimize the termination of the communication interface to provide the best performance. There are two ways to terminate a single-pair Ethernet interface: capacitive coupling or galvanic coupling. Figure 4-1 and Figure 4-2 show simplified versions of the two coupling options.

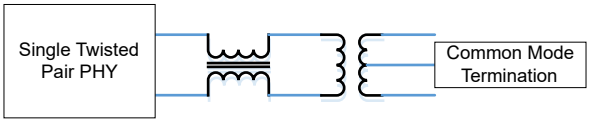

Figure 4-1. Galvanic Decoupling

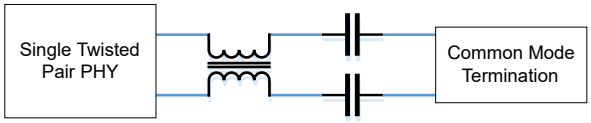

Figure 4-2. Capacitive Decoupling

Given the isolation requirements on the communication line in industrial systems, the rating of the capacitor must be as high as the isolation need. For example, use 1.5kV if building a robot in accordance with the IEC 62368-1 standard.

Comparing the size of the galvanic and the capacitive based coupling for a typical 100Base-T1 implementation, based only on component size is shown in Table 4-1.

Table 4-1. Comparing the Size of Galvanic and Capacitive Coupling Circuits in SPE

Parameter	Galvanic	Capacitive 100V	Capacitive 2kV
Decoupling	28mm^2	36mm^2	144mm^2
Common mode Choke	8mm^2	20mm^2	20mm^2
Common mode Termination	90mm^2	180mm^2	180mm^2
Total	**126mm^2**	236mm^2	344mm^2
Cost comparison normalized price	1.0	0.7	**0.68**
Maximum height of Component used	2.9mm	2.8mm	2.8mm

This summary does not consider coupling of power over dataline (PoDLSPoE) circuits; however, including PoDL does not change much of the analysis from the communication piece of the coupling. The additional circuit of the PoDL coupling can change the result of the analysis. Table 4-1 shows that the size of the components used is not increased by using galvanic coupling – in fact, in the complete circuit, the size of the components is reduced by using galvanic coupling. This analysis is based on components used from Würth electronics. For more details of Würth components for SPE see Single Pair Ethernet.

To compare galvanic and capacitive coupling, two test systems were built to show the performance of each implementation during EMC testing.

During these tests it became clear that galvanic coupling has better performance over capacitive coupling. This is due to capacitor mismatch which makes this circuit more noise sensitive. Also observed was that when with capacitive coupling the Ethernet link was dropped, with galvanic coupling the link was stable with minimal packets lost.

In summary, Texas Instruments (TI) conducted tests on capacitive and galvanic coupling indicating that:

- Galvanic decoupling is less susceptible to noise.
- Galvanic coupling has a better mode conversion loss and return loss performance response than capacitive decoupling, which means that over frequency galvanic coupling attenuates a signal less, thereby improving signal quality and robustness to noise.
- Galvanic tolerances and parasitic effects are more controllable which improves performance when testing against IEC61000-4-x for industrial environments.

In general, if SPE is used in industrial environments, it is most likely necessary to use galvanic coupling to mitigate the poor performance of capacitive coupling observed during EMC system testing and IEC61000-4-x.

Initial tests were conducted which show that galvanic coupling is able to achieve no bit errors to show performance criterion A, during EMC and EMI testing. For further details on these results please contact your local TI representative.

5 Predictive Maintenance in Industrial Environments

Another benefit of some Base-T1 PHYs is the ability to conduct diagnostics of the interface during data communication. Using a diagnostic tool requires a media access control interface to provide full access to the serial management interface of the PHY.

These are the current integrated diagnostic features of the TI PHYs:

- Signal quality indication and cable quality indication
- Time-domain reflectometry
- Electrostatic discharge sensor
- Voltage sensor
- Temperature sensor
- Pseudorandom binary sequence built-in self-test

For more details, see the diagnostic tool kit section of the *DP83TG720S-Q1 1000BASE-T1 Automotive Ethernet PHY with SGMII and RGMII* data sheet.

Base-T1 Ethernet technology features, such as low cable count and high bandwidth, can enable real-time diagnostic capability, including cable diagnostics that can detect when a cable is damaged or degrading. This detection feature allows engineers to replace cables during normal maintenance instead of performing production-line stops.

6 Conclusion

Many of the benefits of the single twisted-pair Ethernet are highly valuable to industrial and robotic applications and can be used to simplify and cost-optimize system functions. The additional diagnostic tools added into the TI Base-T1 PHYs enable new possibilities to achieve predictive maintenance. Base-T1 Ethernet has the potential to be used advantageously in industrial systems, to help enable convergence of IT and OT. Nonetheless, it is important to understand the details impacting system performance for any new technology. This is why TI has conducted tests showing that TI Base-T1 PHYs can support the industrial EMC/EMI requirements, the results of which can be shared upon request. Similarly, organizations like *SPE Industrial Partner Network* and other companies are reviewing the initial hurdles of using the Base-T1 Ethernet interface in industrial environments to understand and improve the technology. TI can support you through these initial hurdles showing initial test results and learning which can quicken the pace using Base-T1 PHYs in industrial systems.

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