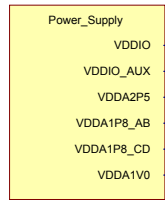
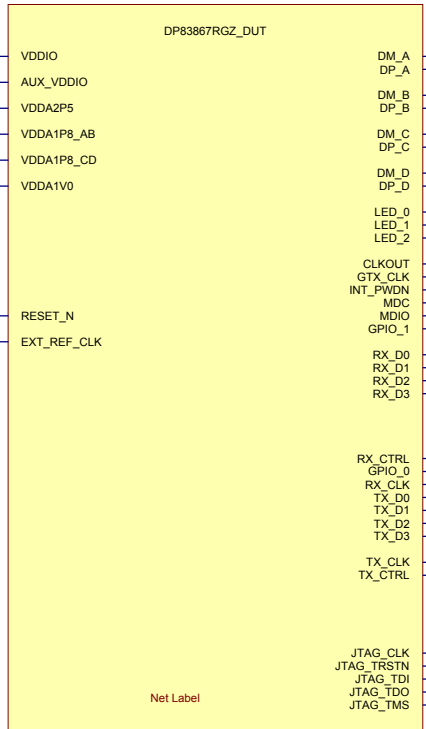


Revision History	
Revision	Notes

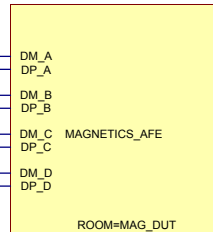
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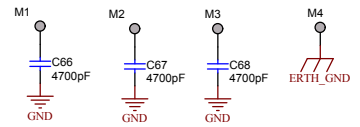
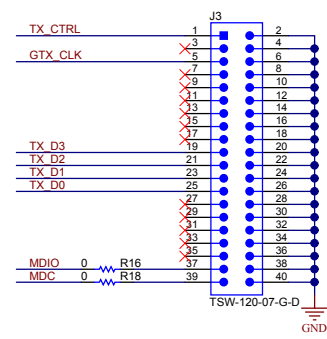
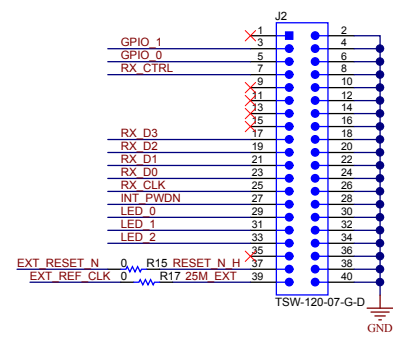
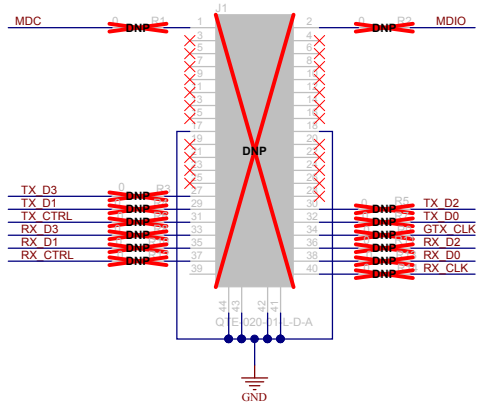
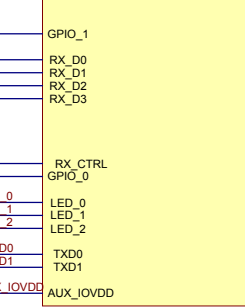
DP83867RGZ DUT



Magnetics



DUT CONFIGURATION

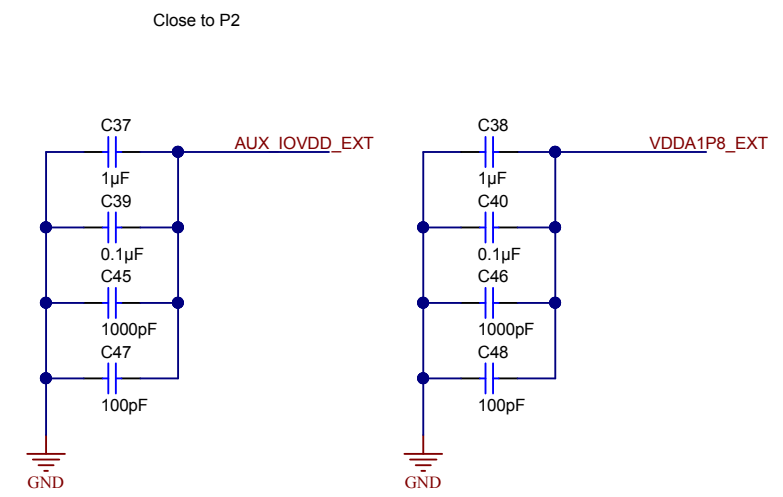
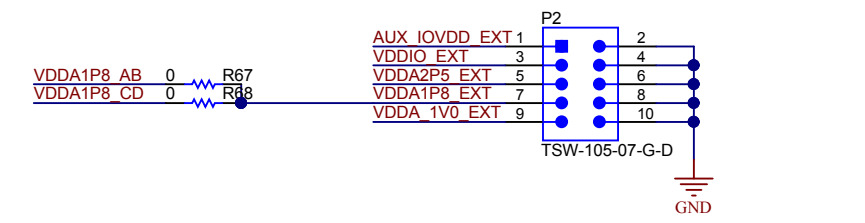
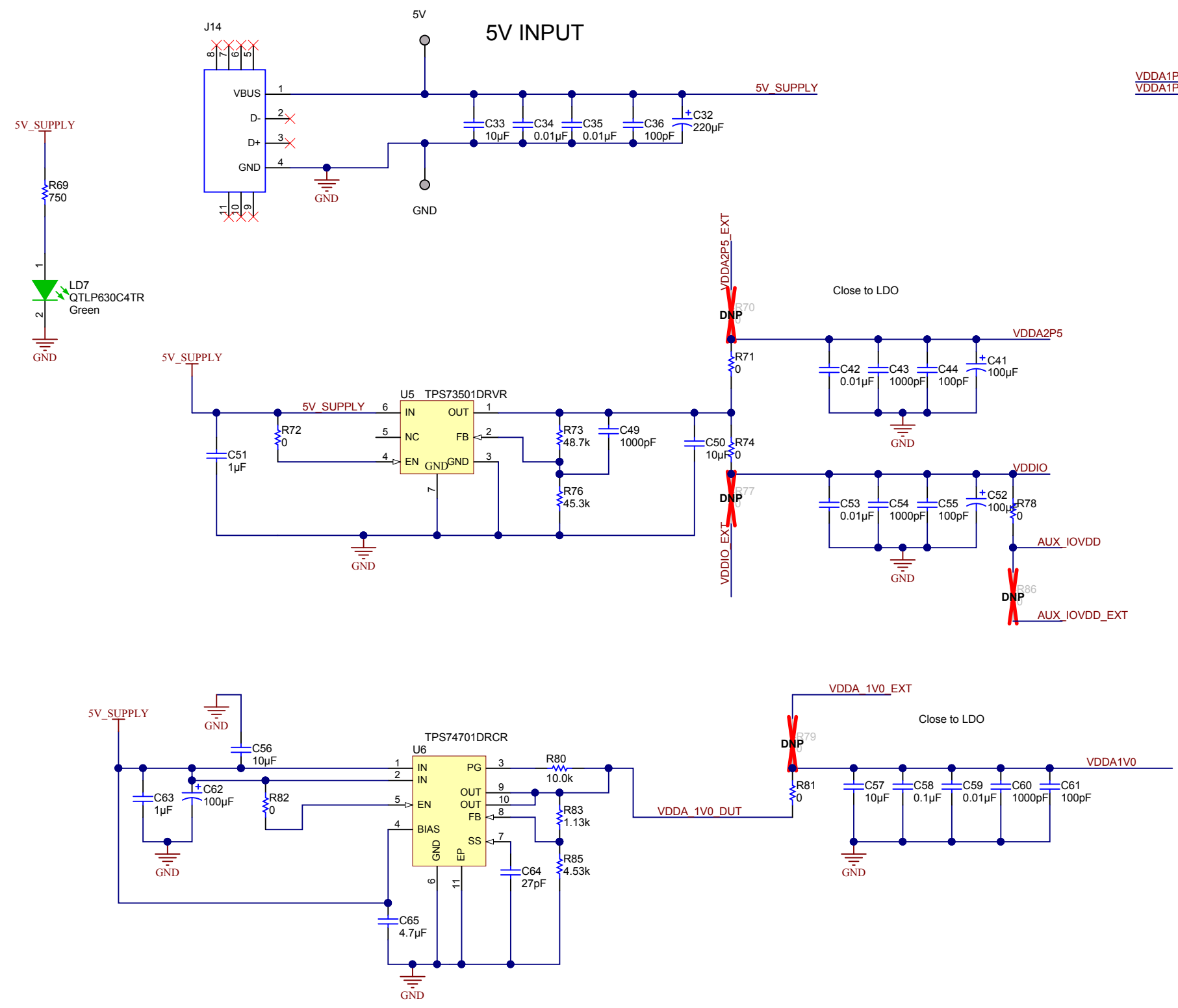


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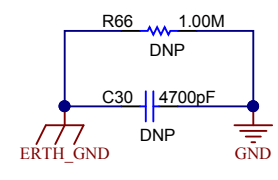
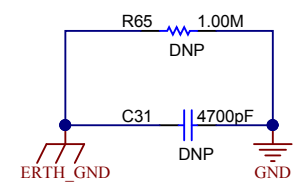
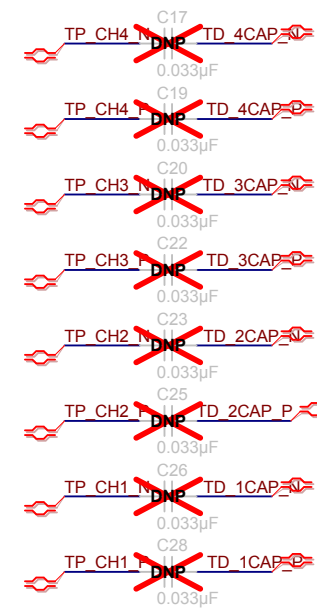
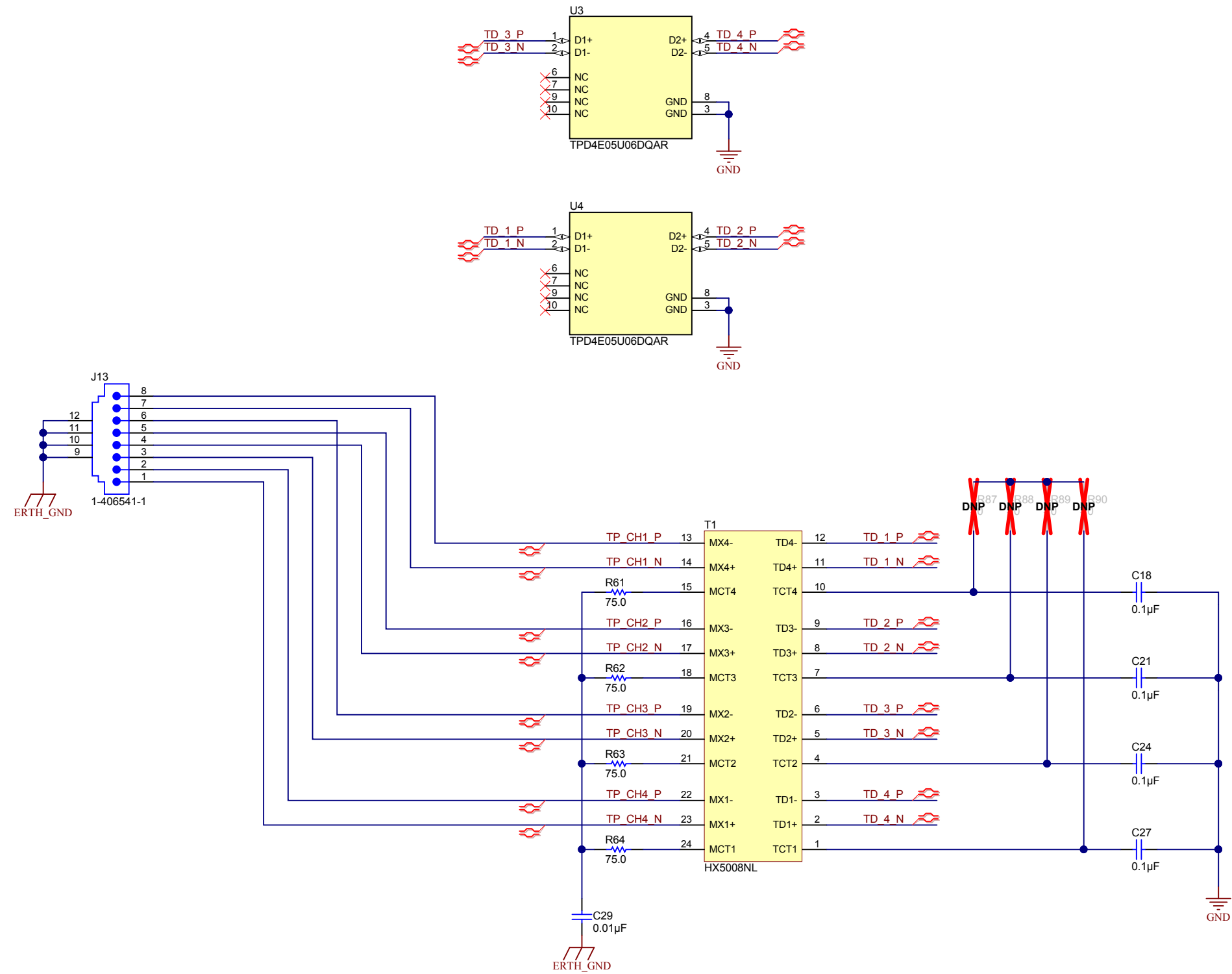
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Drawn By:	File: SV601189A_Block_Diagram_SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	<a href="http://www.ti.com">http://www.ti.com</a>



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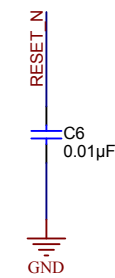
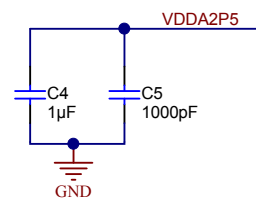
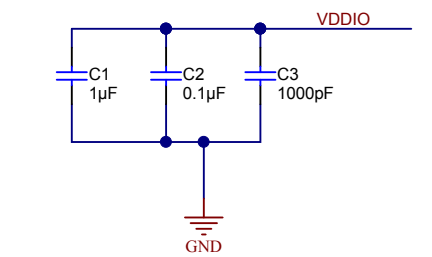
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LBL1  
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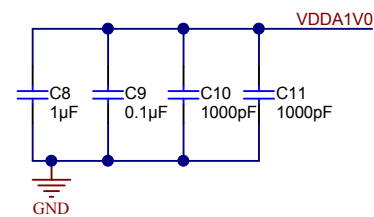
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Drawn By: <a href="#">Aniruddha Khadye</a>	File: <a href="#">SV601189A_Magnetics.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Aniruddha Khadye</a>	Contact: <a href="#">http://www.ti.com/support</a>	

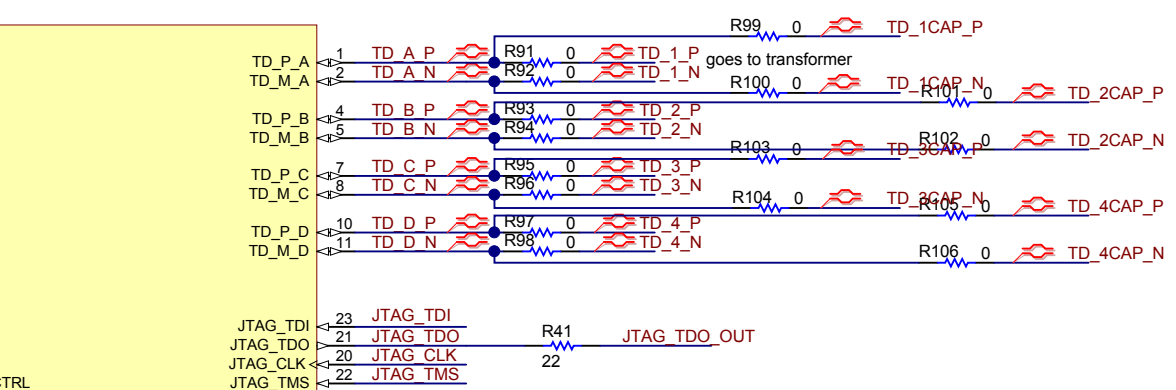
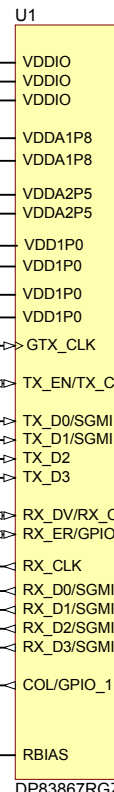
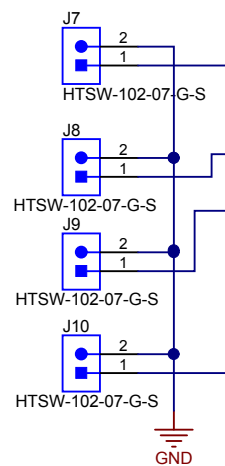
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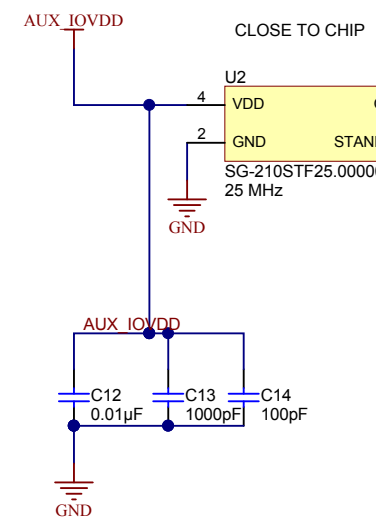
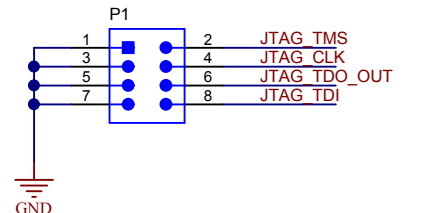
Keep capacitor close to device pin



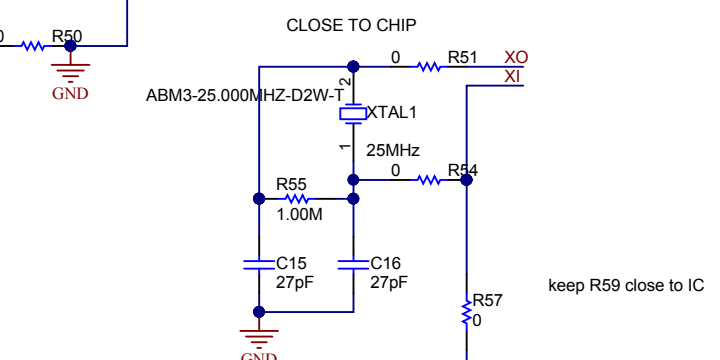
PLACE CLOSE TO CHIP



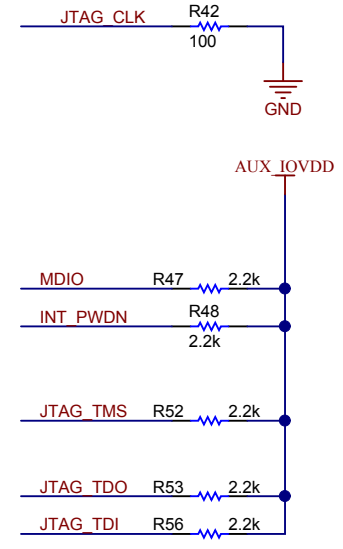
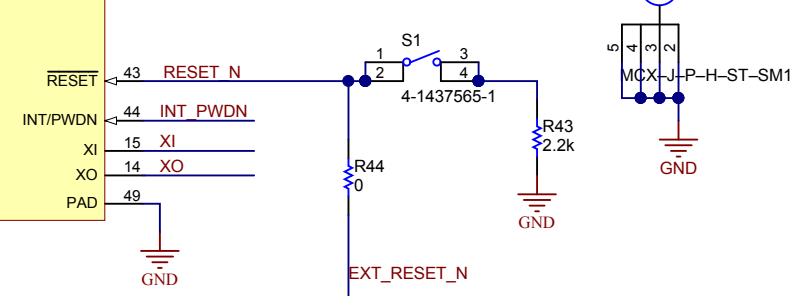
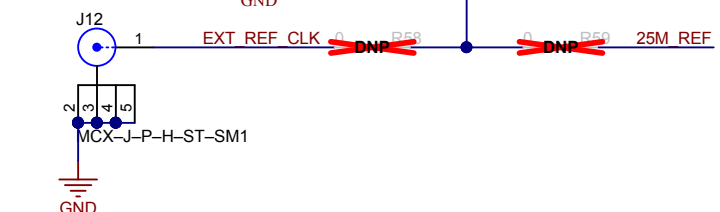
Place trace on inner layers



Place trace on inner layers



keep R59 close to IC

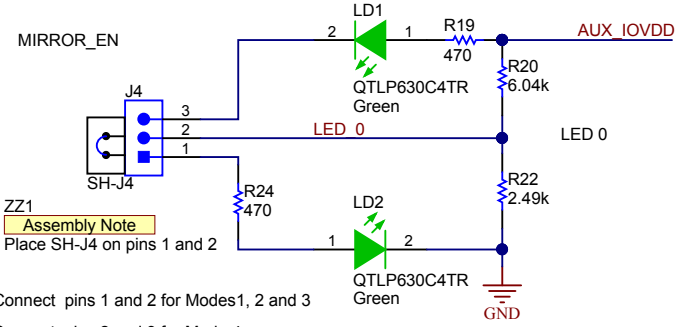


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Drawn By:	File: SV601189A_DP83867ERGZ_SchDoc	Size: B
Engineer: <a href="#">Aniruddha Khadye</a>	Contact: <a href="#">http://www.ti.com/support</a>	

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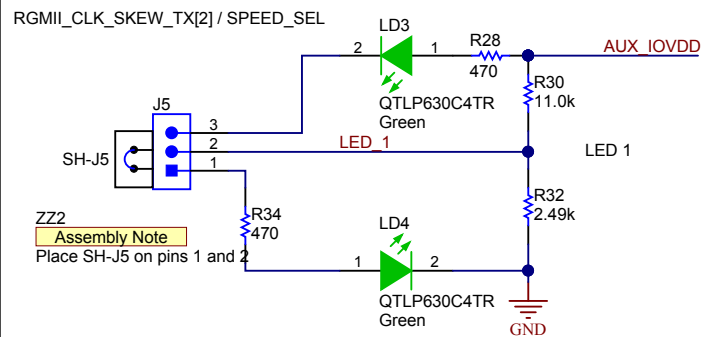
### LED STRAP PINS



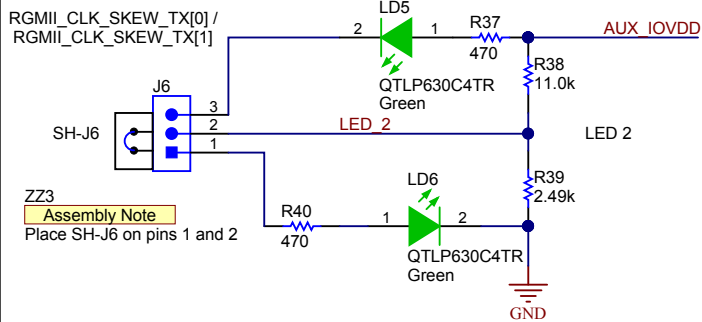
**ZZ1**  
Assembly Note  
Place SH-J4 on pins 1 and 2

Connect pins 1 and 2 for Modes 1, 2 and 3  
Connect pins 2 and 3 for Mode 4

Resistor Values must be changed to change Modes, refer to datasheet for proper values

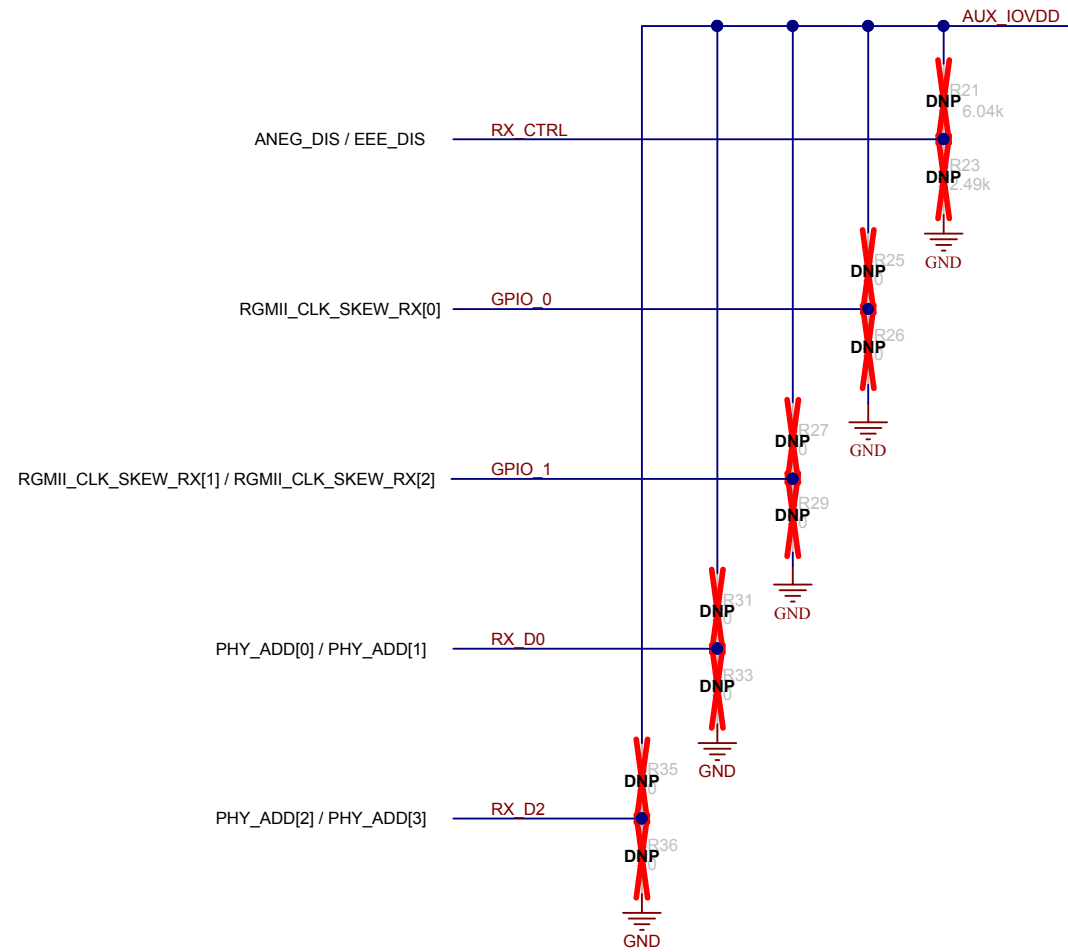


**ZZ2**  
Assembly Note  
Place SH-J5 on pins 1 and 2



**ZZ3**  
Assembly Note  
Place SH-J6 on pins 1 and 2

### CONFIGURATION PINS



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SVN Rev: Version control disabled	Assembly Variant: 001	Engineer: <a href="#">Aniruddha Khadye</a>	Contact: <a href="#">http://www.ti.com/support</a>
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