DSLVDS1001 400-Mbps, Single-Channel LVDS Driver

1 Features

- Designed for signaling rates up to 400-Mbps
- Single 3.3-V Power Supply (3-V to 3.6-V Range)
- 700-ps (100-ps typical) maximum differential skew
- 1.5-ns maximum propagation delay
- Drives small swing (±350-mV) differential signal levels
- Power off protection (Outputs in TRI-STATE)
- Flow-through pinout simplifies PCB layout
- Low power dissipation (23-mW at 3.3 V typical)
- 5-pin SOT-23 package
- Meets or exceeds ANSI TIA/EIA-644-A standard
- Industrial temperature operating range (–40°C to +85°C)

2 Applications

- Board-to-board communication
- Test and measurement
- Motor drives
- LED video walls
- Wireless infrastructure
- Telecom infrastructure
- Multi-function printers
- NIC cards
- Rack servers
- Ultrasound scanners

3 Description

The DSLVDS1001 device is a single-channel, Low-Voltage Differential Signaling (LVDS) driver device designed for applications requiring low power dissipation, low noise, and high data rates. In addition, the short-circuit fault current is also minimized. The device is designed to support data rates that are up to 400-Mbps (200-MHz) using LVDS technology.

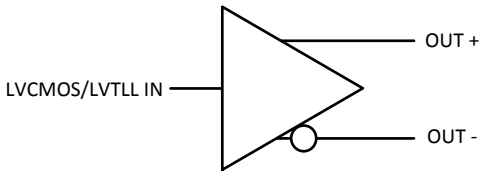
The DSLVDS1001 accepts a 3.3-V LVCMOS/LVTTL input level and outputs low voltage (±350-mV typical) differential signals that have low electromagnetic interference (EMI). The device is in a 5-pin SOT-23 package that is designed for easy PCB layout. The DSLVDS1001 can be paired with its companion single line receiver, the DSLVDS1002, or with any LVDS receiver, to provide a high-speed LVDS interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DSLVDS1001	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram



Typical Application

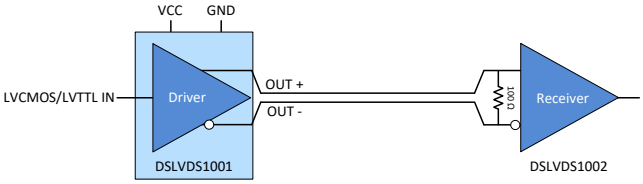


Table of Contents

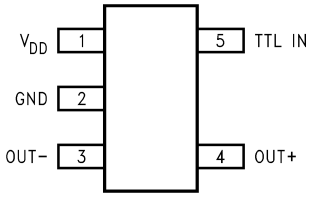
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2018) to Revision A	Page
• Changed device status from: Advanced Information to: Production Data	1
• Added *Documentation Support* section	19

5 Pin Configuration and Functions

DVB Package
5-Pin SOT-23
Top View



(1) See Package Number DBV (R-PDSO-G5)

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Power Supply Pin, +3.3 V ± 0.3 V
2	GND	I	Ground Pin
3	OUT-	O	Inverting Driver Output Pin
4	OUT+	O	Noninverting Driver Output Pin
5	LVCMOS/LVTTL IN	I	LVCMOS/LVTTL Driver Input Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	V_{DD}	–0.3	4	V
LVCMOS input voltage (TTL IN)		–0.3	3.6	V
LVDS output voltage (OUT±)		–0.3	3.9	V
LVDS output short circuit current			24	mA
Lead Temperature – Soldering			260	°C
Maximum Junction Temperature			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±9000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±9000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

6.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD})	3	3.3	3.6	V
Temperature (T_A)	–40	+25	+85	°C

6.4 Thermal Information

THERMAL METRIC(1)		DSLVDS1001 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Over Recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100 Ω (Figure 7) OUT+, OUT– Pins		250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change	R_L = 100 Ω (Figure 8) OUT+, OUT– Pins			3	35	mV
V_{OS}	Offset Voltage	R_L = 100 Ω (Figure 7) OUT+, OUT– Pins		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change	R_L = 100 Ω (Figure 7) OUT+, OUT– Pins				25	mV
I_{OFF}	Power-off Leakage	V_{OUT} = 3.6 V or GND, V_{DD} = 0 V OUT+, OUT– Pins			±2	±15	µA
I_{OS}	Output Short Circuit Current(3)	V_{OUT+} and V_{OUT-} = 0 V OUT+, OUT– Pins			−5	−20	mA
I_{OSD}	Differential Output Short Circuit Current(3)	V_{OD} = 0 V OUT+, OUT– Pins			−5	−12	mA
V_{IH}	Input High Voltage	TTL IN Pin		2		V_{DD}	V
V_{IL}	Input Low Voltage	TTL IN Pin		GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3 V or 2.4 V TTL IN Pin			±2	±15	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5 V TTL IN Pin			±2	±15	µA
C_{IN}	Input Capacitance	TTL IN Pin			3		pF
I_{DD}	Power Supply Current	No Load	V_{IN} = V_{DD} or GND		5	8	mA
		R_L = 100 Ω	V_{IN} = V_{DD} or GND		7	10	

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{DD} = +3.3 V and T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

6.6 Switching Characteristics

Over Recommended Supply Voltage and Operating Temperature Ranges, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 15 pF	0.5	1	1.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	(Figure 9 and Figure 10)	0.5	1.1	1.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(5)		0	0.1	0.7	ns
t_{SKD4}	Differential Part to Part Skew(6)		0	0.4	1.2	ns
t_r	Rise Time		0.2	0.5	1	ns
t_f	Fall Time		0.2	0.5	1	ns
f_{MAX}	Maximum Operating Frequency(7)		200	250		MHz

(1) All typicals are given for: V_{DD} = +3.3 V and T_A = +25°C.
(2) These parameters are specified by design, and not tested in production. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(3) C_L includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns (10%-90%).
(5) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD2}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(7) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, V_{OD} > 250 mV. The parameter is specified by design. The limit is based on the statistical analysis of the device over the PVT range by the transitions times (t_{TLH} and t_{THL}).

6.7 Typical Characteristics

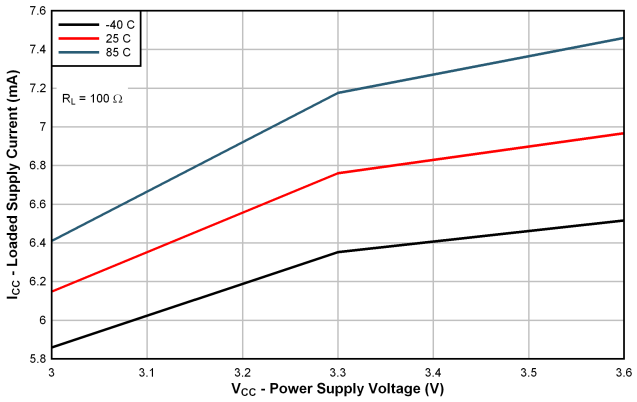


Figure 1. Loaded Supply Current vs Power Supply Voltage

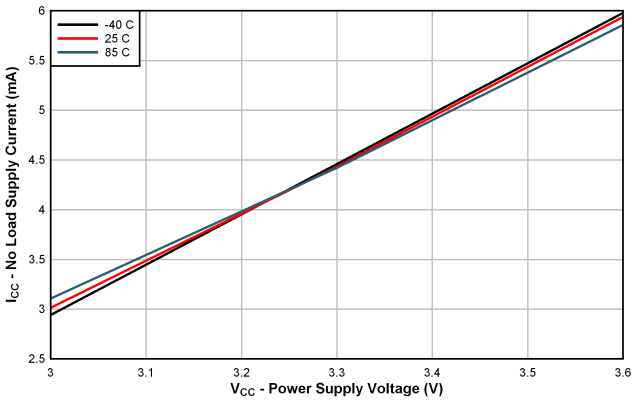


Figure 2. No Load Supply Current vs Power Supply Voltage

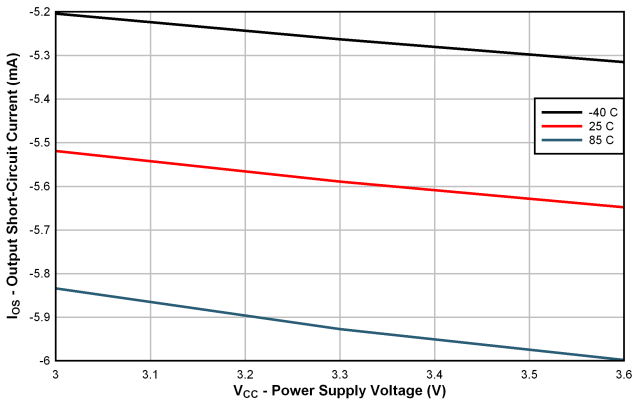


Figure 3. Output Short-Circuit Current vs Power Supply Voltage

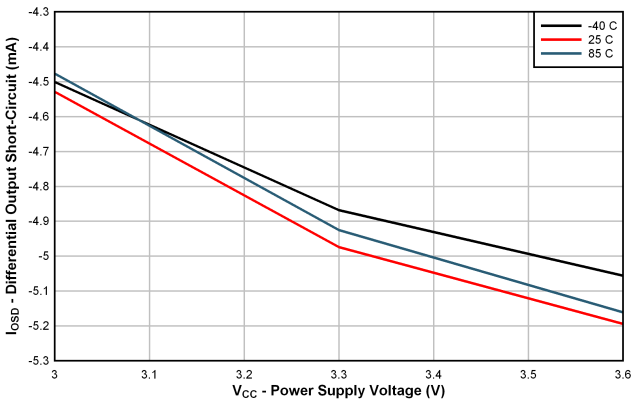


Figure 4. Differential Output Short-Circuit Current vs Power Supply Voltage

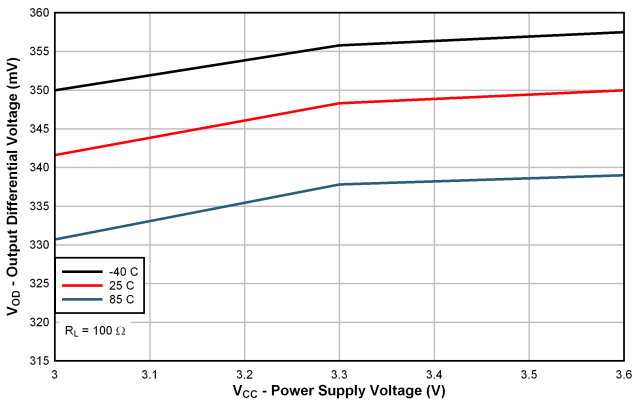


Figure 5. Output Differential Voltage vs Power Supply Voltage

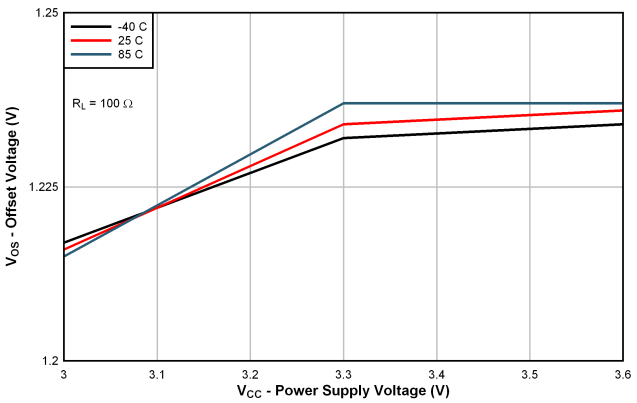


Figure 6. Offset Voltage vs Power Supply Voltage

7 Parameter Measurement Information

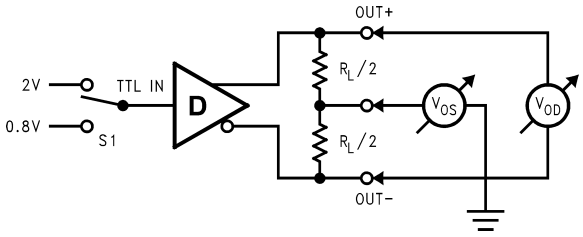


Figure 7. Differential Driver DC Test Circuit

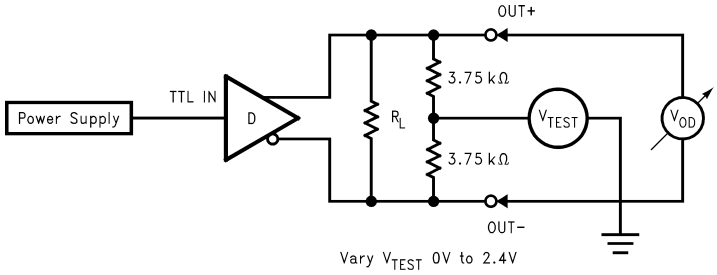


Figure 8. Differential Driver Full Load DC Test Circuit

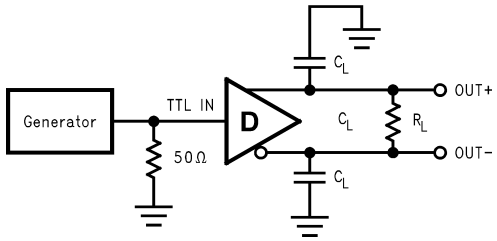


Figure 9. Differential Driver Propagation Delay and Transition Time Test Circuit

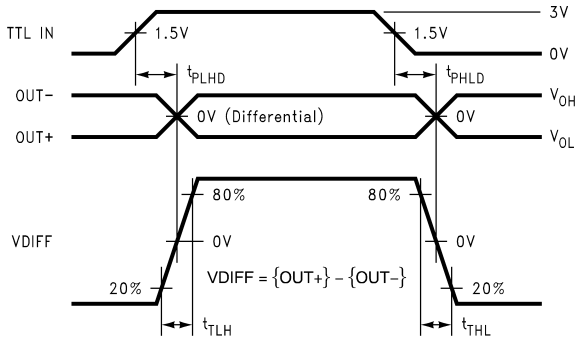


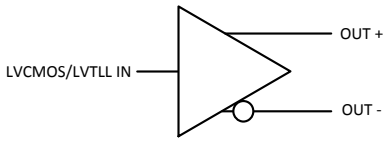
Figure 10. Differential Driver Propagation Delay and Transition Time Waveforms

8 Detailed Description

8.1 Overview

The DSLVDS1001 device is a single-channel, low-voltage differential signaling (LVDS) line driver. It operates from a single supply that is nominally 3.3-V, but can be as low as 3-V and as high as 3.6-V. The input signal to the DSLVDS1001 is an LVCMOS/LVTTL signal. The output of the device is a differential signal complying with the LVDS standard (TIA/EIA-644). The differential output signal operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in low emmsions durning electromagnetic compatability (EMC) testing. The differential nature of the output provides immunity to common-mode coupled signals that the driven signal may experience. The DSLVDS1001 device is intended to drive a 100-Ω transmission line. This transmission line may be a printed-circuit board (PCB) or cabled interconnect. With transmission lines, the optimum signal quality and power delivery is reached when the transmission line is terminated with a load equal to the characteristic impedance of the interconnect. Likewise, the driven 100-Ω transmission line should be terminated with a matched resistance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DSLVDS1001 Driver Functionality

As can be seen in Table 1, the driver single-ended input to differential output relationship is defined. When the driver input is left open, the differential output is undefined.

Table 1. DSLVDS1001 Driver Functionality

INPUT	OUTPUTS	
LVCMOS/LVTTL IN	OUT +	OUT -
H	H	L
L	L	H
Open	?	?

8.3.2 Driver Output Voltage and Power-On Reset

The DSLVDS1001 driver operates and meets all the specified performance requirements for supply voltages in the range of 3 V to 3.6 V. When the supply voltage drops below 1.5-V (or is turning on and has not yet reached 1.5-V), power-on reset circuitry set the driver output to a high-impedance state.

8.3.3 Driver Offset

An LVDS-compliant driver is required to maintain the common-mode output voltage at 1.2 V (±75 mV). The DSLVDS1001 incorporates sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 3-V to 3.6-V supply range.

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DSLVDS1001 device is a single-channel LVDS driver. The functionality of this device is simple, yet extremely flexible, leading to its use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below.

9.2 Typical Application

9.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 11.

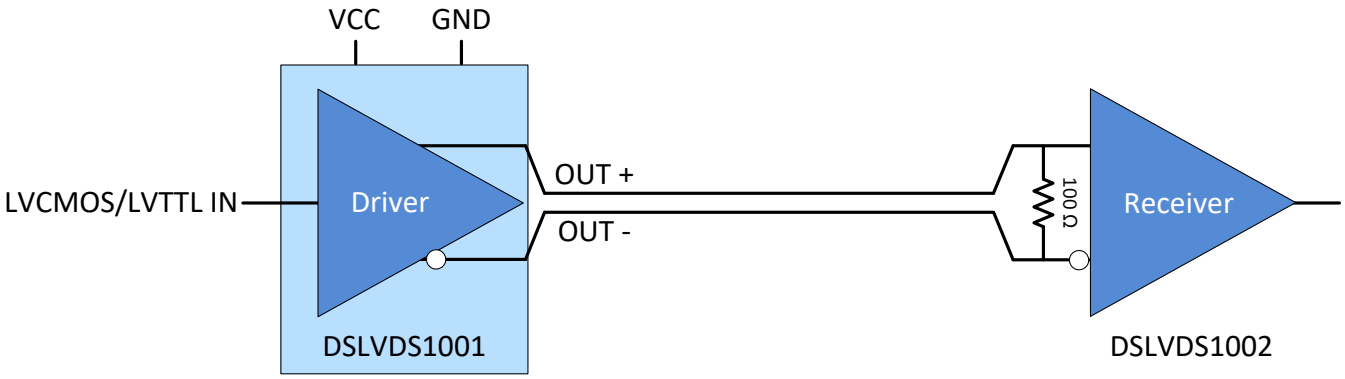


Figure 11. Typical Application

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 11, the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

9.3 Design Requirements

Table 2 shows the design parameters for this example.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CC})	3 to 3.6 V
Driver Input Voltage	0 to 3.6 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Ground shift between driver and receiver	±1 V

9.4 Detailed Design Procedure

9.4.1 Driver Supply Voltage

The DSLVDS1001 driver is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The driver output voltage is dependent upon the chosen supply voltage. The minimum output voltage stays within the specified LVDS limits (247 mV to 450 mV) for a 3.3 V supply. If the supply range is between 3 V and 3.6 V, the minimum output voltage may be as low as 150 mV. If a communication link is designed to operate with a supply within this lower range, the channel noise margin must be looked at carefully to ensure error-free operation.

9.4.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson[(1)], equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV. This figure varies, however, depending on the noise budget available in the design. [(1)]

$$C_{chip} = \left(\frac{\Delta I_{Maximum\ Step\ Change\ Supply\ Current}}{\Delta V_{Maximum\ Power\ Supply\ Noise}} \right) \times T_{Rise\ Time} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

Figure 12 lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). Place the smallest value of capacitance as close to the chip as possible.

Figure 12. Recommended LVDS Bypass Capacitor Layout

9.4.3 Driver Input Voltage

The DSLVDS1001 input is designed to support a wide input voltage range. The input stage can accept signals as high as 3.6 V.

9.4.4 Driver Output Voltage

The DSLVDS1001 driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 350 mV. This 350 mV is the absolute value of the differential swing (V_{OD} = $|V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 700 mV.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

Detailed Design Procedure (continued)

In this example, the LVDS receiver thresholds are ±100 mV. With these receiver decision thresholds, it is clear that the disadvantage of operating the driver with a lower supply will be noise margin. With fully-compliant LVDS drivers and receivers, TI expects a minimum noise margin of approximately 150 mV (247-mV minimum output voltage – 100-mV maximum input requirement). If the DSLVDS1001 operates within the 3 V to 3.6 V supply range, the minimum noise margin will drop to 150 mV.

9.4.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, with the key points included here. This media may be a twisted pair, a twinax cable, a flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with a variation no more than 10% (90 Ω to 132 Ω).

9.4.6 PCB Transmission Lines

As per the *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187), Figure 13 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure has a signal line and a return path with a uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure and the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 13 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent (like when S is less than 2W, for example), the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

Detailed Design Procedure (continued)

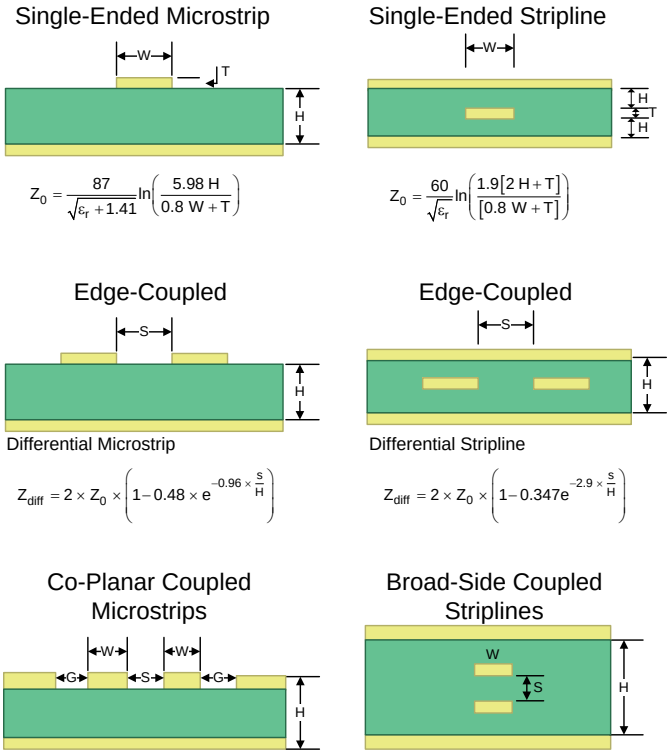


Figure 13. Controlled-Impedance Transmission Lines

9.4.7 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line that is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 Ω and 110 Ω.

The line termination resistance should be placed as close to the receiver as possible to minimize the stub length from the resistor to the receiver.

Remember to only place line termination resistors at the end(s) of the transmission line in these multidrop topologies.

9.5 Application Curve

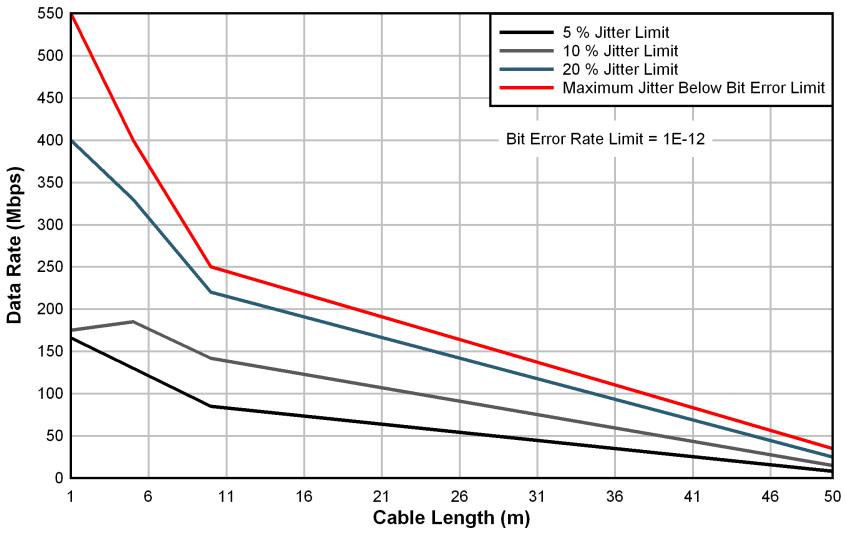


Figure 14. DSLVDS1001 Performance: Data Rate vs Cable Length

10 Power Supply Recommendations

10.1 Power Supply Considerations

The DSLVDS1001 driver is designed to operate from a single power supply with supply voltage in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per the *LVDS Application and Data Handbook* (SLLD009), printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 15.

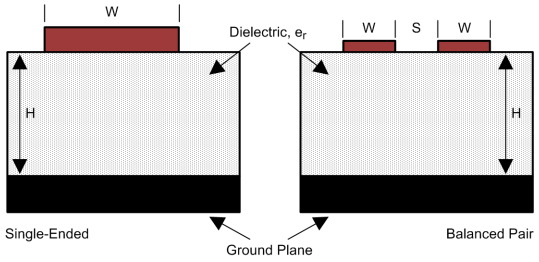


Figure 15. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(2), 2(3), and 3(4) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (2) (3) (4)

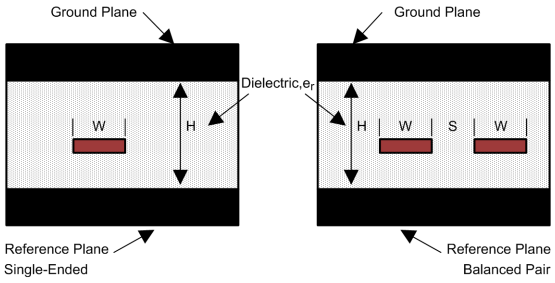


Figure 16. Stripline Topology

(2) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(3) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(4) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. When the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 17.

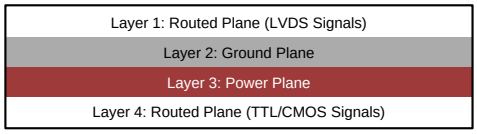


Figure 17. Four-Layer PCB

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 18.

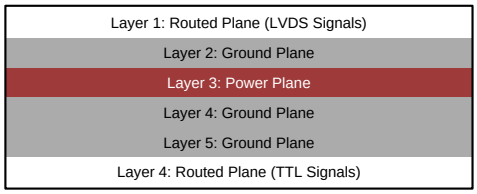


Figure 18. Six-Layer PCB

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity, but fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces can depend on several factors, but the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

Layout Guidelines (continued)

In the case of two adjacent single-ended traces, one should use the 3-W rule: the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

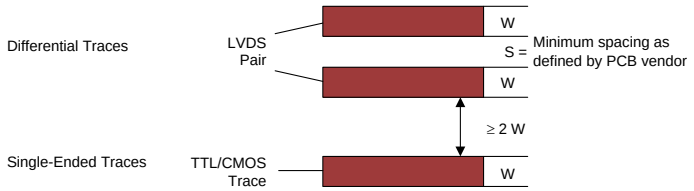


Figure 19. 3-W Rule for Single-Ended and Differential Traces (Top View)

NOTE

Exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

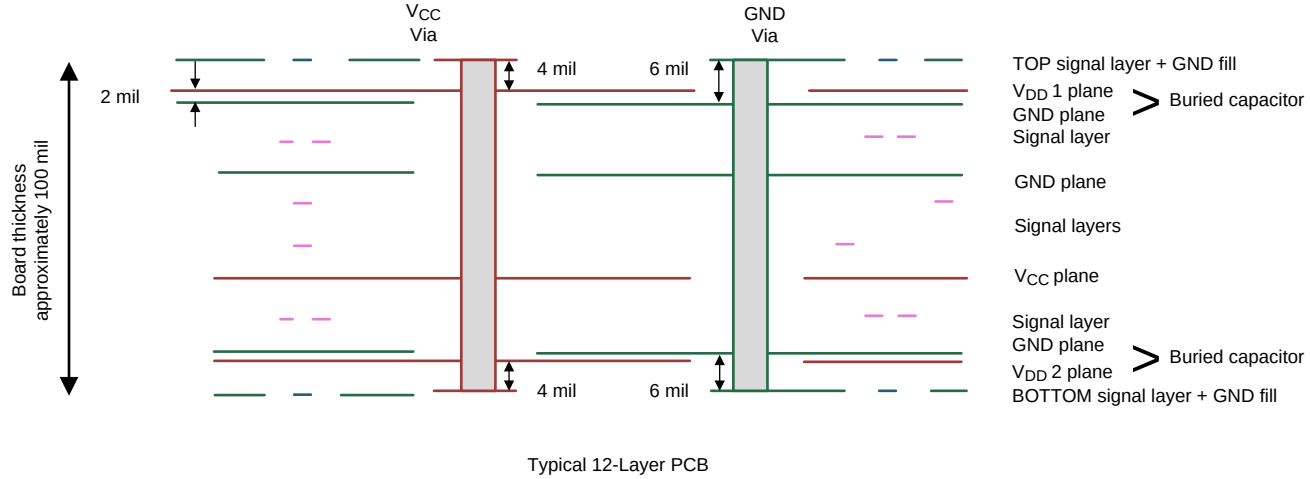


Figure 20. Low-Inductance, High-Capacitance Power Connection

Layout Guidelines (continued)

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 21(a).

An X7R surface-mount capacitor of size 0402 has about 0.5-nH body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 13 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 13) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases, the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 21(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

Figure 21. Typical Decoupling Capacitor Layouts

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 22.

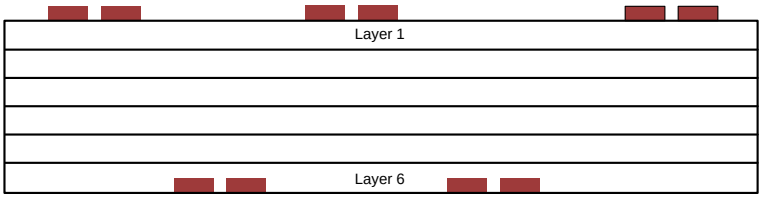


Figure 22. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers. Thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends that the designer have an adjacent ground via for every signal via, as shown in Figure 23. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

Layout Guidelines (continued)

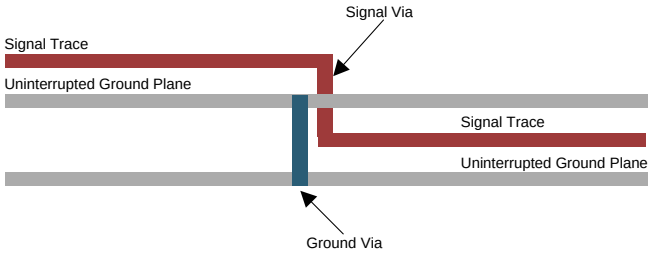


Figure 23. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11.2 Layout Example

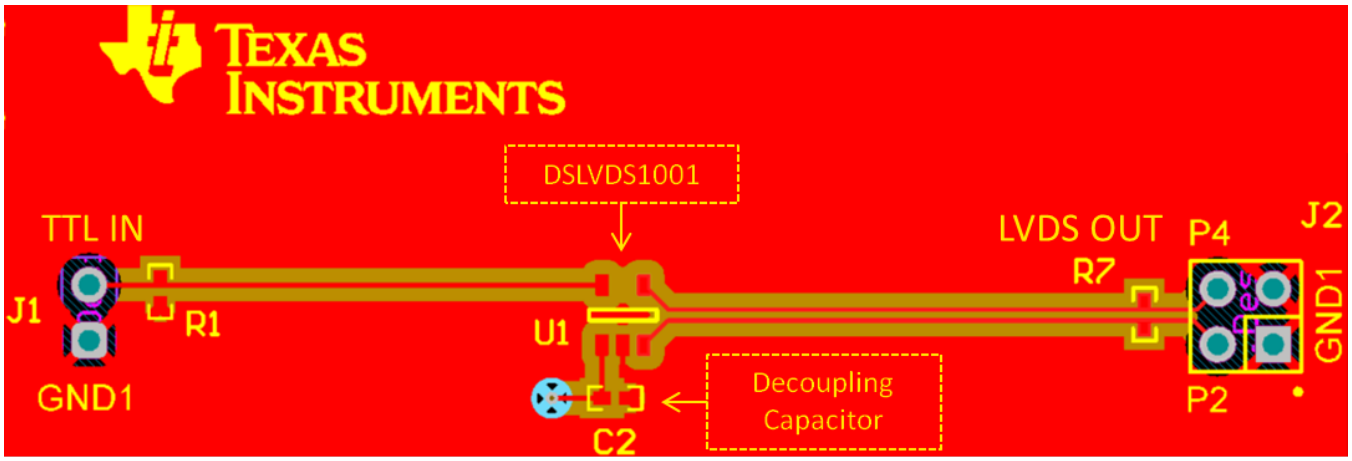


Figure 24. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *AN-1194 Failsafe Biasing of LVDS Interfaces* (SNLA051)
- *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187)
- *LVDS Application and Data Handbook* (SLLD009)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DSLVDS1001DBVR	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	1TBX	
DSLVDS1001DBVT	LIFEBUY	SOT-23	DBV	5	250	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	1TBX	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

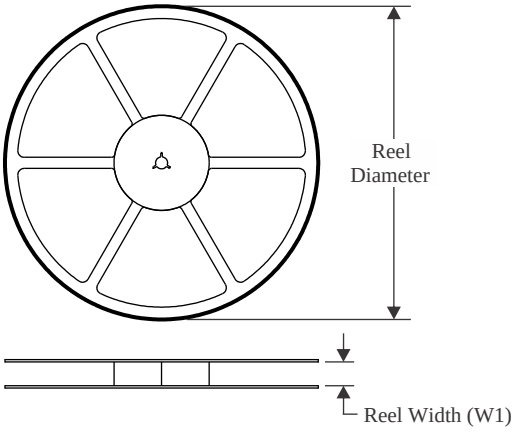
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

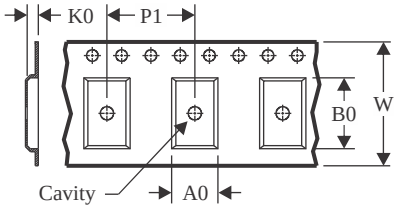
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

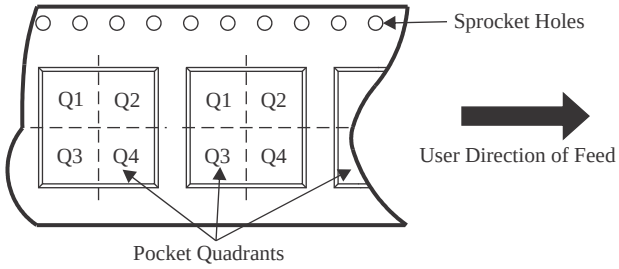


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

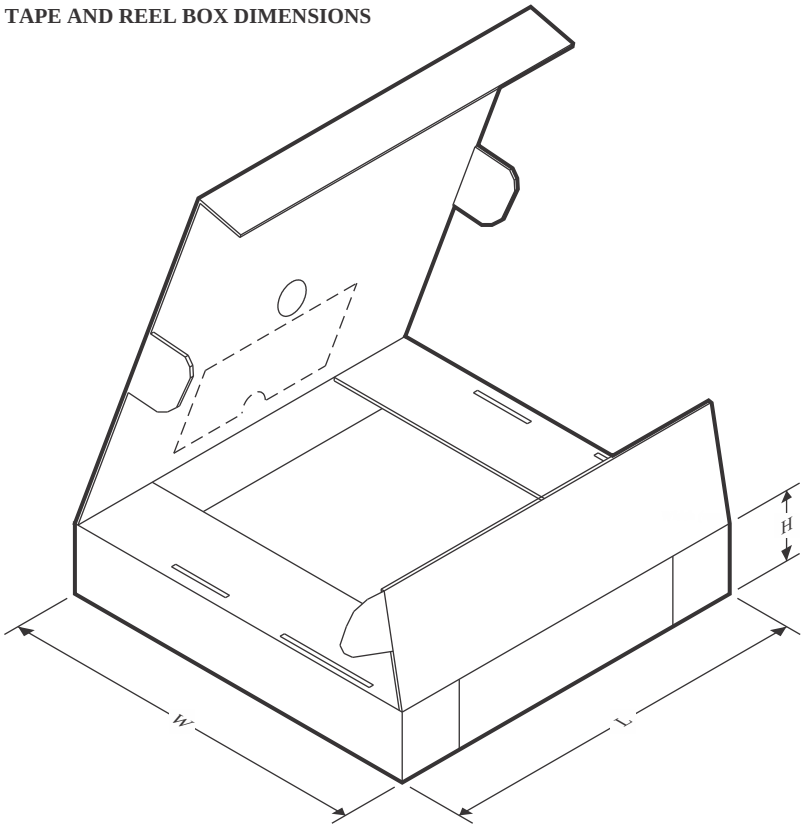
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DSLVDS1001DBVR	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DSLVDS1001DBVT	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

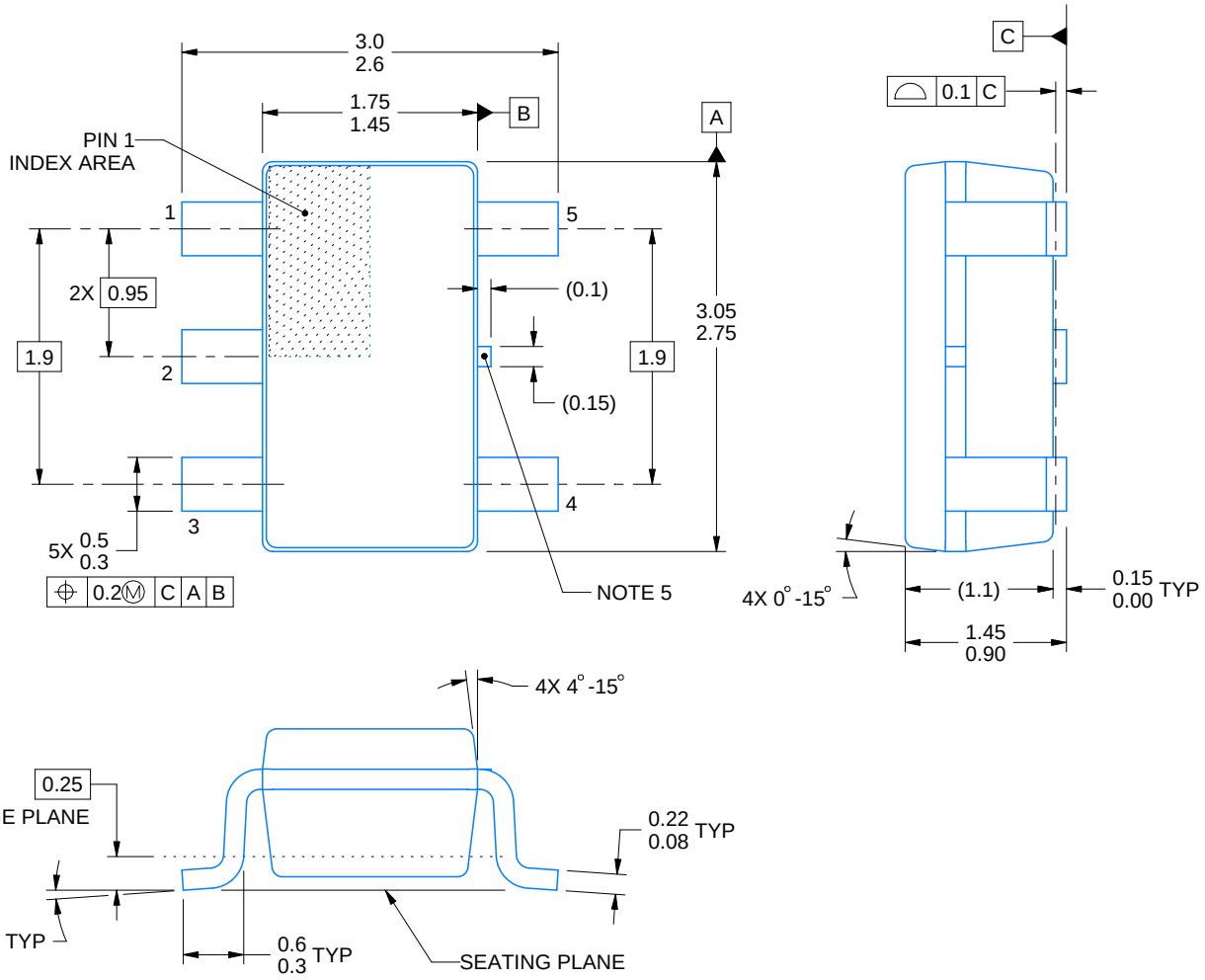
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DSLVDS1001DBVR	SOT-23	DBV	5	1000	210.0	185.0	35.0
DSLVDS1001DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

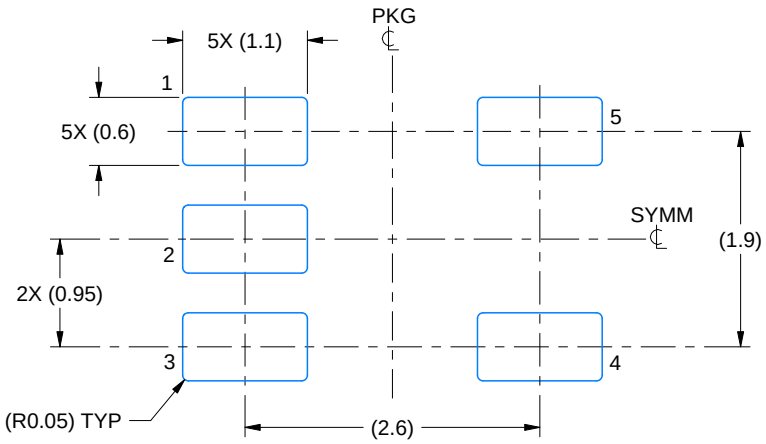
SMALL OUTLINE TRANSISTOR



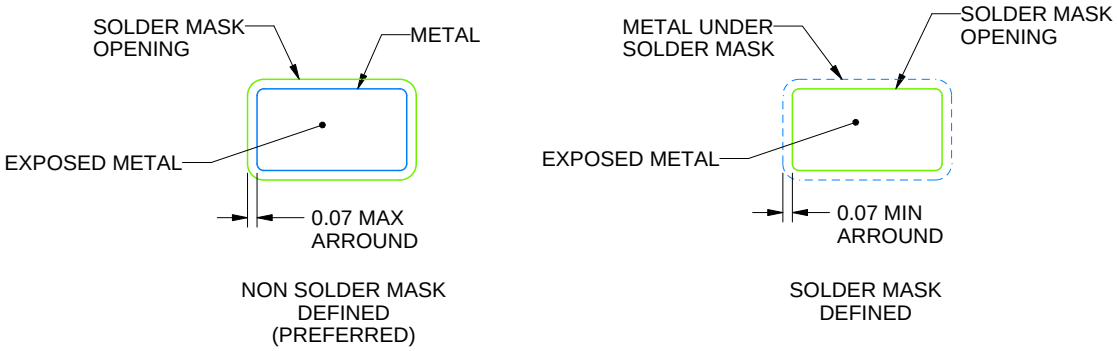
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

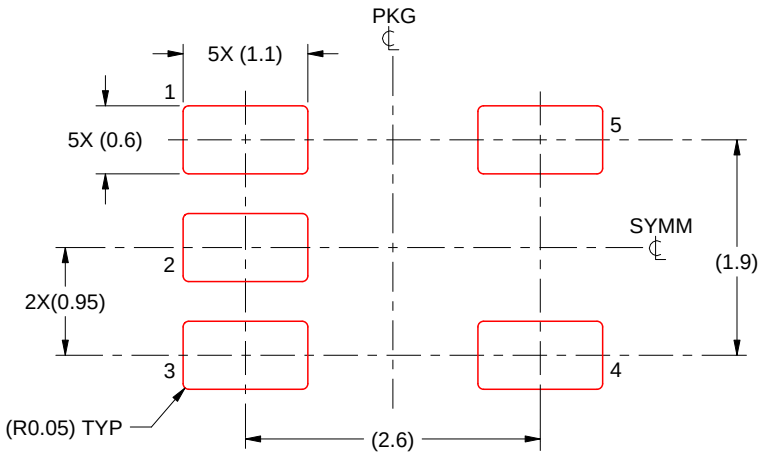


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265