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AN-1416 LP3991TL DSBGA Evaluation Board Information

1 Introduction

This board is designed to allow the evaluation of the LP3991 low voltage CMOS regulator. Each board is pre-assembled and tested in the factory. The board contains the LP3991 in a 4 bump DSBGA package and input and output capacitors connected to GND . The LP3991 is capable of operating with an input voltage as low as 1.65 V for output voltage options of 1.5 V or less. The LP3991 can supply a maximum output current of 300 mA and is particularly suitable for powering digital circuits, where good transient behavior is required. It can be employed in applications requiring post regulation of switching regulators to provide maximum efficiency in battery powered products.

2 Operation

The input voltage, applied between V_{IN} and GND should be at least 0.5 V above the output voltage with a minimum of 1.65 V and a maximum of 3.3 V. For output voltages of 1.5 V or higher, the LP3991 will operate with an input voltage of only 0.2 V above V_{OUT}. However, some loss in performance of PSSR and transient behavior can be expected when operating the device with such a low V_{IN} to V_{OUT} difference. Input connections should be kept reasonably short (<300 mm) to minimize input inductance and ensure optimum transient performance. If longer leads are used, then it may be required to increase the input capacitor value to 2.2 µF or 4.7 µF.

ON/OFF control of the LP3991 is provided on the evaluation board by a logic signal applied to the V_{EN} pin. A minimum of 0.95 V is required to ensure the device to be on and the device will be shutdown with V_{EN} set to 0.4 V or less. If ON/OFF control is not required, the V_{EN} pin can be connected to V_{IN}. The evaluation board has provision for an optional link (R1) for this purpose.

A load can be connected from the V_{OUT} pin to GND.

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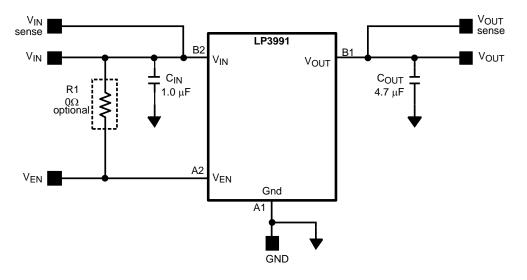## 3 Schematic Diagram

The schematic is shown in Figure 1.

Figure 1. Evaluation Board Schematic
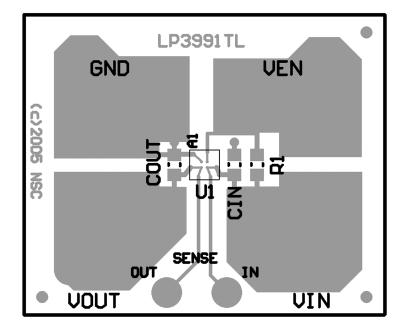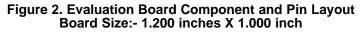
4 PCB Layout

The board layout is shown in Figure 2.

Figure 2. Evaluation Board Component and Pin Layout
Board Size:- 1.200 inches X 1.000 inch

Table 1. Bill of Materials (BOM) for LP3991 DSBGA Evaluation Board

Item	Value	Qty	Footprint	Notes
U1	LP3991-X.X	1	YZR0004	"X.X" corresponds to the output voltage option.
C_{IN}	1.0µF	1	0603	X5R, Input Capacitor
C_{OUT}	4.7µF	1	0603	X5R, Output Capacitor
R1	0Ω	Not Fitted	0805	Connects V_{IN} to V_{EN}
Test Pins		4		

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