User's Guide

LM5149-Q1 Buck Converter Evaluation Module User's Guide

ABSTRACT

With an input operating voltage as low as 3.5 V and up to 100 V as specified in Table 1-1, the LM514x-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability, and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI, and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF). All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

Table 1-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC Controller	Single or Dual	V_{IN} Range	Control Method	Gate Drive Voltage	Sync Output	EMI Mitigation
LM25141-Q1	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM25143-Q1	Dual	3.5 V to 42 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM25148-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS
LM25149-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS, AEF
LM5141-Q1	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143-Q1	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM5145-Q1	Single	5.5 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5146-Q1	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5148-Q1	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS
LM5149-Q1	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS, AEF

The LM5149-Q1EVM-400 evaluation module (EVM) is a synchronous buck DC/DC regulator that employs synchronous rectification to achieve high conversion efficiency in a small footprint. It operates over a wide input voltage range of 15 V to 72 V, providing a regulated output of 12 V. The output voltage has better than 1% setpoint accuracy and is adjusted by modifying the feedback resistor values, permitting the user to customize the output voltage as needed.

The LM5149-Q1 synchronous buck controller used in the EVM has the following features:

- Wide input voltage (wide V_{IN}) range of 3.5 V to 80 V
- Spread spectrum modulation and active EMI filtering for lower EMI
- Wide duty cycle range with low $t_{ON(min)}$ and $t_{OFF(min)}$
- Ultra-low shutdown and no-load standby quiescent currents
- Multiphase capability
- Peak current-mode control loop architecture
- Integrated, high-current MOSFET gate drivers
- Cycle-by-cycle overcurrent protection with hiccup
- Functional-safety capable

The free-running switching frequency of the EVM is 400 kHz and is synchronizable to a higher or lower frequency, if required. Moreover, a synchronization output signal (SYNCOUT) 180° phase-shifted relative to the internal clock is available for dual-phase leader-follower configurations. VCC and gate drive UVLO protects the regulator at low input voltage conditions, and EN pins for each channel support application-specific power-up and power-down requirements.

The LM5149-Q1 is available in a 24-pin VQFN package with 5.5-mm × 3.5-mm footprint to enable DC/DC solutions with high density and low component count. See the *LM5149-Q1 3.5-V to 80-V Synchronous Buck DC/DC Controller Data Sheet* for more information. Use the LM5149-Q1 with the WEBENCH® Power Designer to create a custom regulator design. To optimize component selection and examine predicted efficiency performance across line and load ranges, download the *LM5149-Q1 Quickstart Calculator*.

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1 High Density EVM Description

The LM5149-Q1EVM-400 high-density EVM is designed to use a regulated or non-regulated high-voltage input rail ranging from 15 V to 72 V to produce a tightly regulated output voltage of 12 V at load currents up to 8 A. This wide V_{IN} range DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The free-running switching frequency is 400 kHz and is synchronizable to an external clock signal at a higher or lower frequency. The power-train passive components selected for this EVM, including buck inductors and ceramic input and output capacitors, are automotive AEC-Q200 rated and are available from multiple component vendors.

1.1 Typical Applications

- High-current automotive electronic systems
- ADAS and body electronics
- Infotainment systems and instrument clusters
- Automotive HEV/EV powertrain systems

1.2 Features and Electrical Performance

- Wide input voltage operating range of 15 V to 72 V
- 1% accurate fixed 12 V, 5 V, 3.3 V, or adjustable output down to 0.8 V
- Switching frequency of 400 kHz externally synchronizable up or down by 20%
- Full-load efficiency of 95% at V_{IN} = 48 V
- 55-µA controller standby current at V_{IN} = 48 V
- Optimized for ultra-low EMI
  - Dual-random spread spectrum and active EMI filtering
  - Meets CISPR 25 and UNECE Reg 10 EMI standards
- Peak current-mode control architecture provides fast line and load transient response
  - Integrated slope compensation adaptive with switching frequency
  - Forced PWM (FPWM) or pulsed-frequency modulation (PFM) operation
  - Optional internal or external loop compensation
- Integrated high-side and low-side power MOSFET gate drivers
  - 2.2-A and 3.2-A sink and source gate drive current capability
  - 13-ns adaptive dead-time control reduces power dissipation and MOSFET temperature rise
- Overcurrent protection (OCP) with hiccup mode for sustained overload conditions
- SYNCOUT signal 180° out-of-phase with internal clock
- Power Good signal with 100-kΩ pullup resistor to VCC
- Internal 3-ms soft start
- Fully assembled, tested, and proven PCB layout with 83-mm × 43-mm total footprint

2 EVM Characteristics

Table 2-1 lists the electrical characteristics.

Table 2-1. Electrical Performance Characteristics

Parameter	Test Conditions		MIN	TYP	MAX	Unit
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		15	48	72	V
Input current, no load, I_{IN-NL}	I_{OUT} = 0 A, PFM tied to VDDA, UVLO removed	V_{IN} = 24 V		84		µA
		V_{IN} = 48 V		55		
		V_{IN} = 72 V		46		
Input current, shutdown, I_{IN-OFF}	V_{EN} = 0 V	V_{IN} = 48 V		3		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} (1)			11.88	12	12.12	V
Output current, I_{OUT}	V_{IN} = 15 V to 72 V, Airflow = 100 LFM(2)		0		8	A
Output voltage regulation, ΔV_{OUT}	Load regulation	I_{OUT} = 0 A to 8 A		0.1%		
	Line regulation	V_{IN} = 15 V to 72 V		1%		
Output voltage ripple, V_{OUT-AC}	V_{IN} = 48 V, I_{OUT} = 8 A			12		mVrms
Output overcurrent protection, I_{OCP}	V_{IN} = 48 V			10		A
Soft-start time, t_{SS}				3		ms
SYSTEM CHARACTERISTICS						
Switching frequency, F_{SW-nom}	V_{IN} = 48 V			400		kHz
PFM Light-load efficiency, η_{LIGHT} (1)	I_{OUT} = 1 A	V_{IN} = 24 V		94.8%		
		V_{IN} = 48 V		90.5%		
		V_{IN} = 60 V		89.1%		
Half-load efficiency, η_{HALF}	I_{OUT} = 4 A	V_{IN} = 24 V		97.0%		
		V_{IN} = 48 V		95.1%		
		V_{IN} = 60 V		94.1%		
Full load efficiency, η_{FULL}	I_{OUT} = 8 A	V_{IN} = 24 V		96.2%		
		V_{IN} = 48 V		95.4%		
		V_{IN} = 60 V		94.9%		
LM5149-Q1 junction temperature, T_J			–40		150	°C

(1) The default output voltage of this EVM is 12 V. Efficiency and other performance metrics can change based on operating input voltage, load currents, externally-connected output capacitors, and other parameters.
(2) The recommended airflow when operating at input voltages greater than 60 V is 100 LFM.

3 Application Circuit Diagram

Figure 3-1 shows the schematic of an LM5149-Q1-based synchronous buck regulator with an active EMI filter.

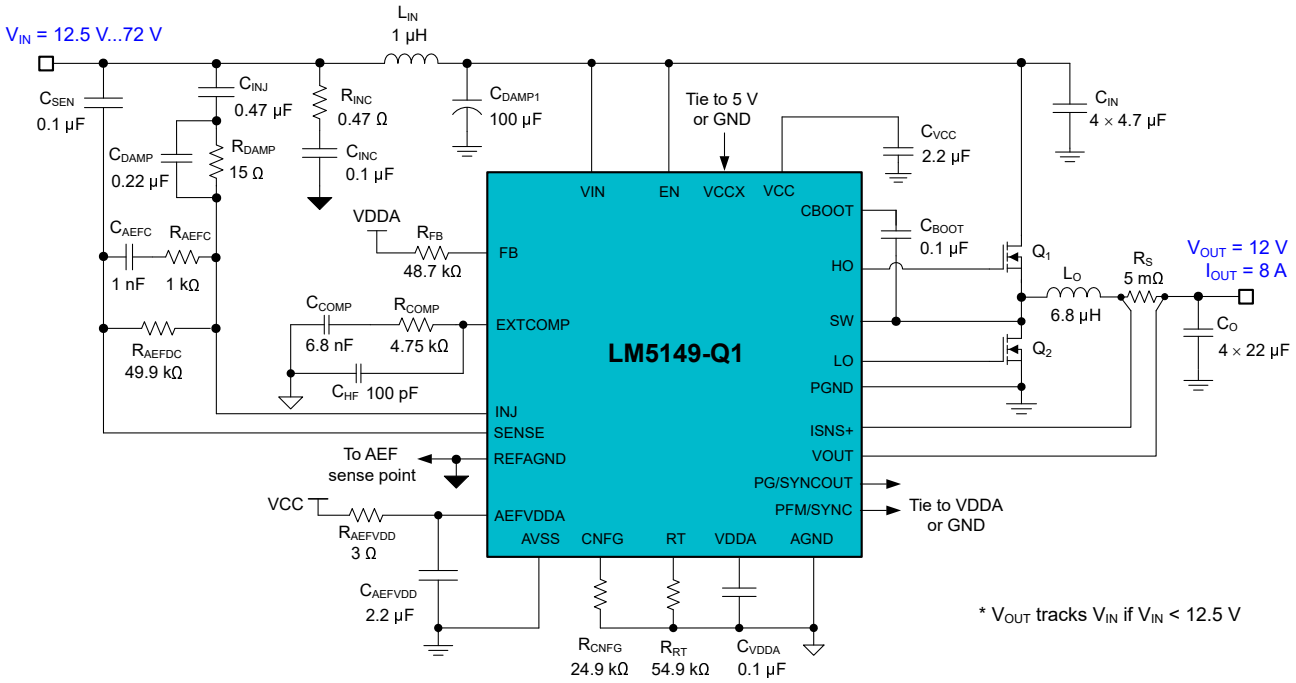


Figure 3-1. LM5149-Q1 Synchronous Buck Regulator Simplified Schematic

4 EVM Photo

Figure 4-1 shows the EVM photo.

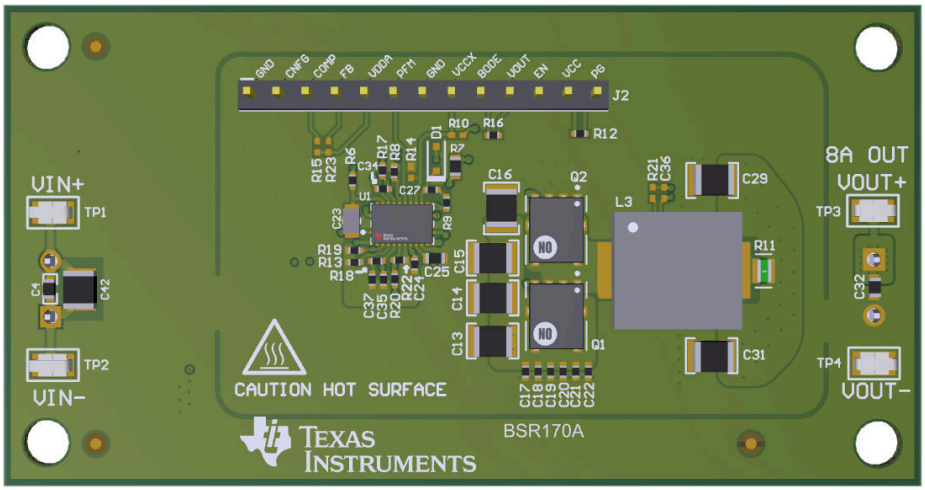


Figure 4-1. LM5149-Q1 EVM Photo, 83 mm × 43 mm

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

5 Test Setup and Procedure

5.1 EVM Connections

Referencing the EVM connections described in Table 5-1, the recommended test setup to evaluate the LM5149-Q1EVM-400 is shown in Figure 5-1. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before handling the EVM.

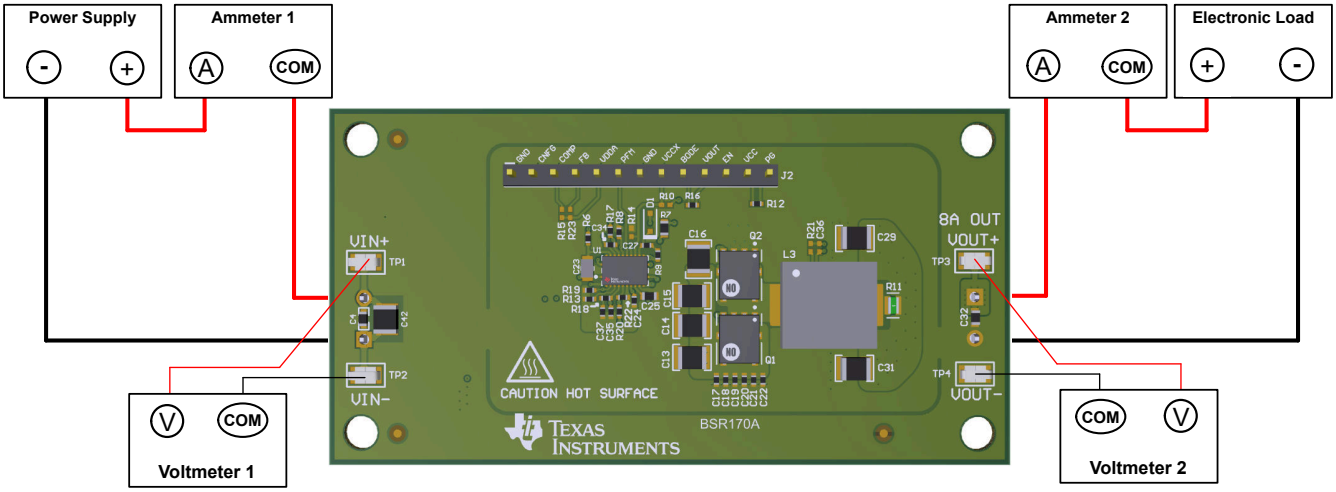


Figure 5-1. EVM Test Setup

CAUTION

Refer to the LM5149-Q1 data sheet, LM5149-Q1 Quickstart Calculator, and WEBENCH® Power Designer for additional guidance pertaining to component selection and controller operation.

Table 5-1. EVM Power Connections

LABEL	DESCRIPTION
VIN+	Positive input voltage power and sense connection
VIN–	Negative input voltage power and sense connection
VOUT+	Positive output voltage power and sense connection
VOUT–	Negative output voltage power and sense connection

Table 5-2. EVM Signal Connections

LABEL	DESCRIPTION
GND	GND connection
CNFG	Configuration input - tie to GND to disable AEF
COMP	Error amplifier output
FB	FB node
VDDA	Bias supply connection for the analog circuits
PFM	PFM/FPWM selection and Synchronization input
GND	GND connection
VCCX	Optional external VCC bias supply for higher efficiency
BODE	50-Ω injection point for loop response
VOUT	Output voltage
EN	ENABLE input – tie to GND to disable the device
VCC	Bias supply connection for the gate drivers and AEF
PGOOD	Power Good indicator

5.2 Test Equipment

Voltage Source: Use an input voltage source capable of supplying 0 V to 80 V and 12 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set the voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT to GND. Set the voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set the ammeter to 1-second aperture time.
- **Ammeter 2:** Output current. Set the ammeter to 1-second aperture time.

Electronic Load: The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 A_{DC} to 10 A_{DC} at 12 V. For a no-load input current measurement, disconnect the electronic load as it can draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that may be live or energized.

5.3 Recommended Test Setup

5.3.1 Input Connections

1. Prior to connecting the DC input source, set the current limit of the input supply to 0.1 A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 5-1.
2. Connect voltmeter 1 at VIN+ and VIN– connection points to measure the input voltage.
3. Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

5.3.2 Output Connections

1. Connect electronic load to VOUT connection. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
2. Connect voltmeter 2 at VOUT and GND connections to measure the output voltage.
3. Connect ammeter 2 to measure the output current.

5.4 Test Procedure

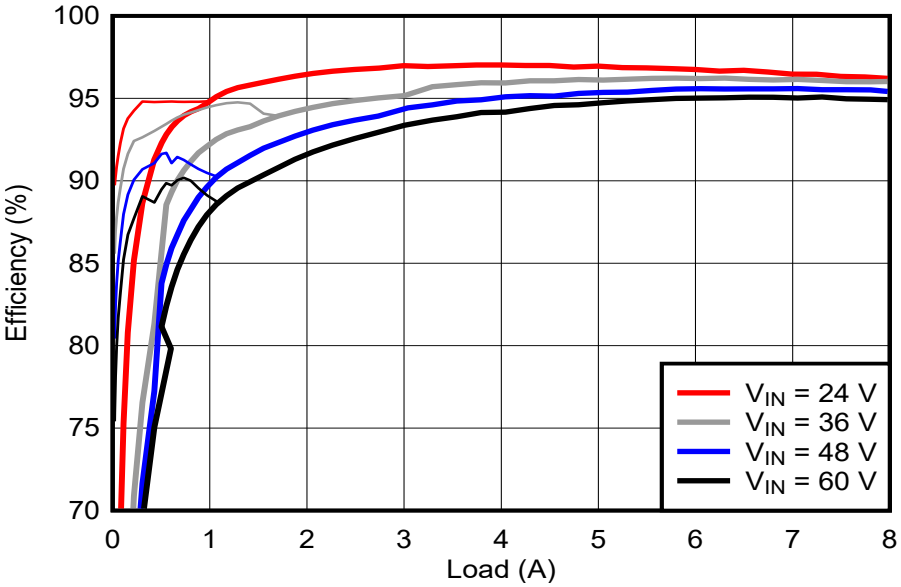
5.4.1 Line and Load Regulation, Efficiency

1. Set up the EVM as previously described.
2. Set the load to constant resistance or constant current mode and to sink 0 A.
3. Increase input source from 0 V to 48 V; use voltmeter 1 to measure the input voltage.
4. Increase the current limit of the input supply to 12 A.
5. Using voltmeter 2 to measure the output voltage, V_{OUT}, vary the load current from 0 A to 8 A_{DC}; V_{OUT} must remain within the load regulation specification.
6. Set the load current to 4 A (50% rated load) and vary the input source voltage from 15 V to 72 V; V_{OUT} must remain within the line regulation specification.
7. Decrease load to 0 A. Decrease input source voltage to 0 V.

6 Test Data and Performance Curves

Figure 6-1 through Figure 6-14 present typical performance curves for the LM5149-Q1EVM-400. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

6.1 Conversion Efficiency



The curves with higher efficiency at light load correspond to when diode emulation is enabled (PFM tied to VDDA).

Figure 6-1. Efficiency,V_{IN} = 48 V, V_{OUT} = 12 V

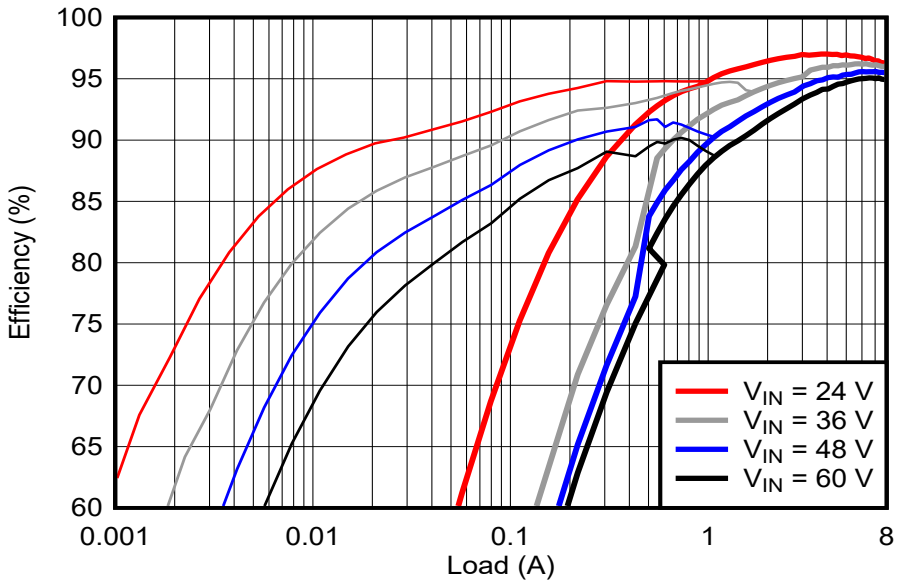


Figure 6-2. Efficiency, V_{IN} = 48 V, V_{OUT} = 12 V, Log Scale

6.2 Operating Waveforms

6.2.1 Switching

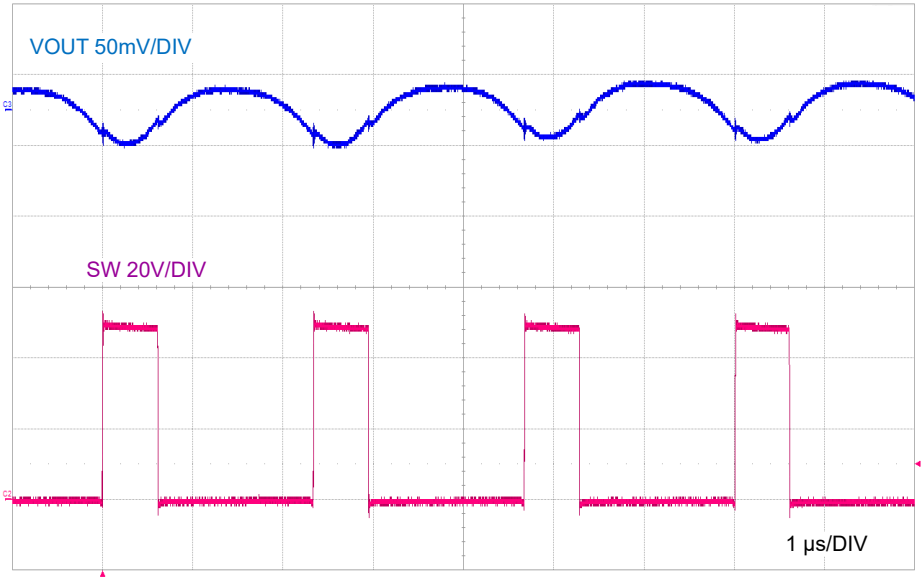


Figure 6-3. Steady State Operation, V_{IN} = 48 V, I_{OUT} = 8 A

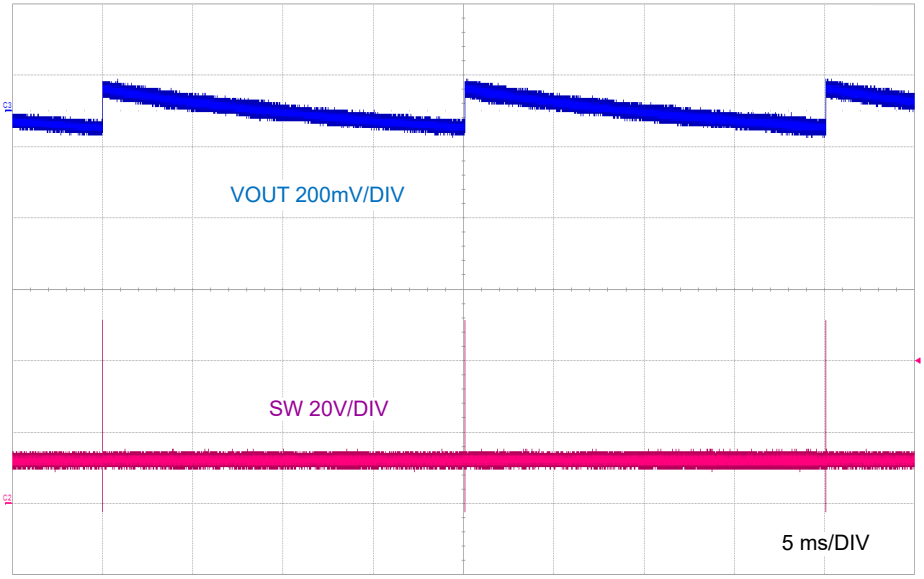


Figure 6-4. Steady State Operation in PFM Mode, V_{IN} = 48 V, I_{OUT} = 0 A

6.2.2 Load Transient Response

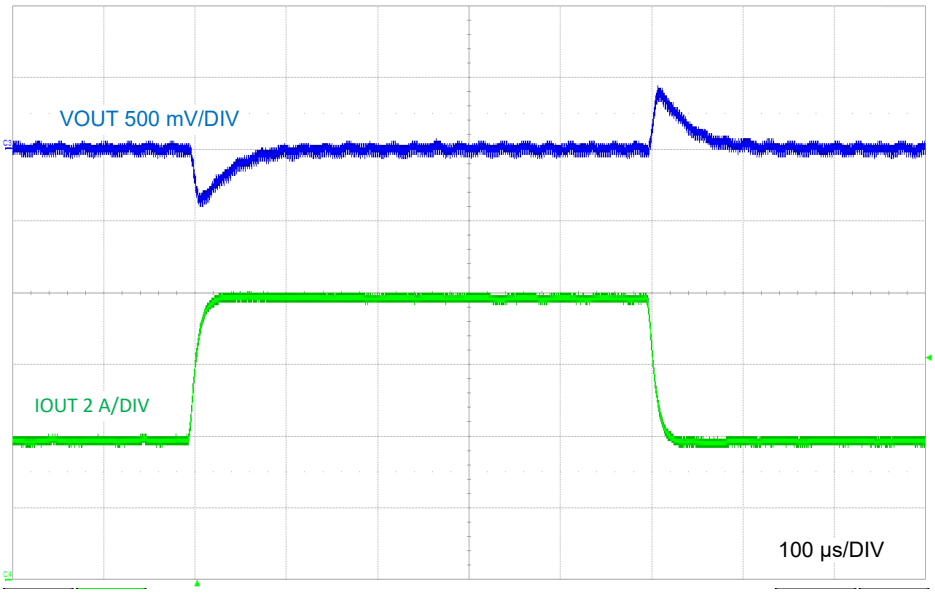


Figure 6-5. Load Transient Response, V_{IN} = 48 V, FPWM, 4 A to 8 A at 1 A/µs

6.2.3 Line Transient Response

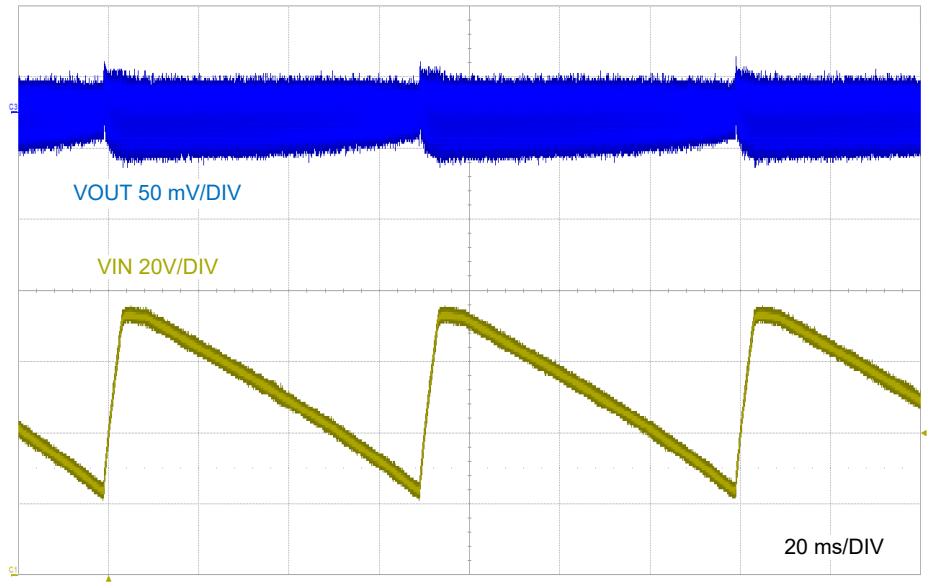


Figure 6-6. Line Transient Response to V_{IN} = 24 V to 72 V, I_{OUT} = 4 A

6.2.4 Start-Up and Shutdown With EN

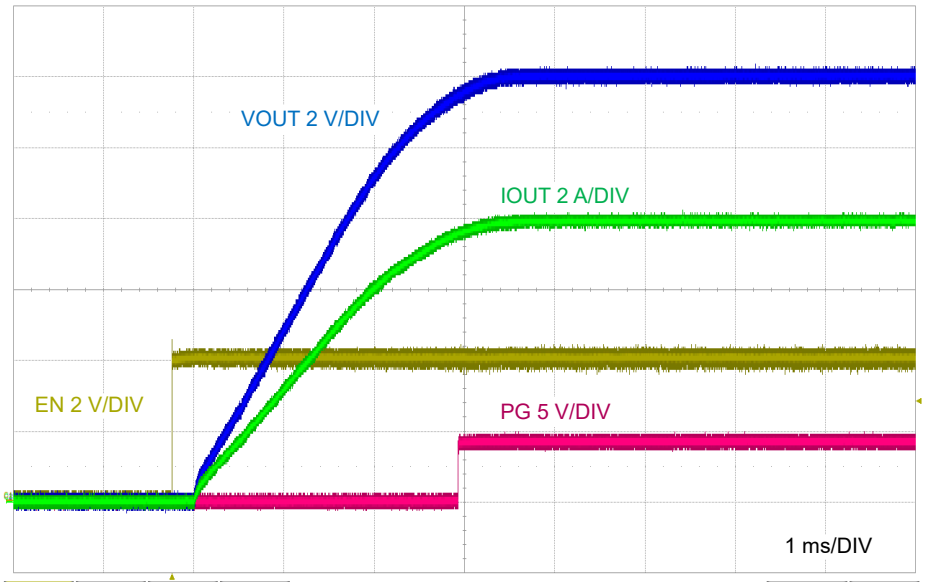


Figure 6-7. EN ON, V_{IN} = 48 V, I_{OUT} = 8-A Resistive Load

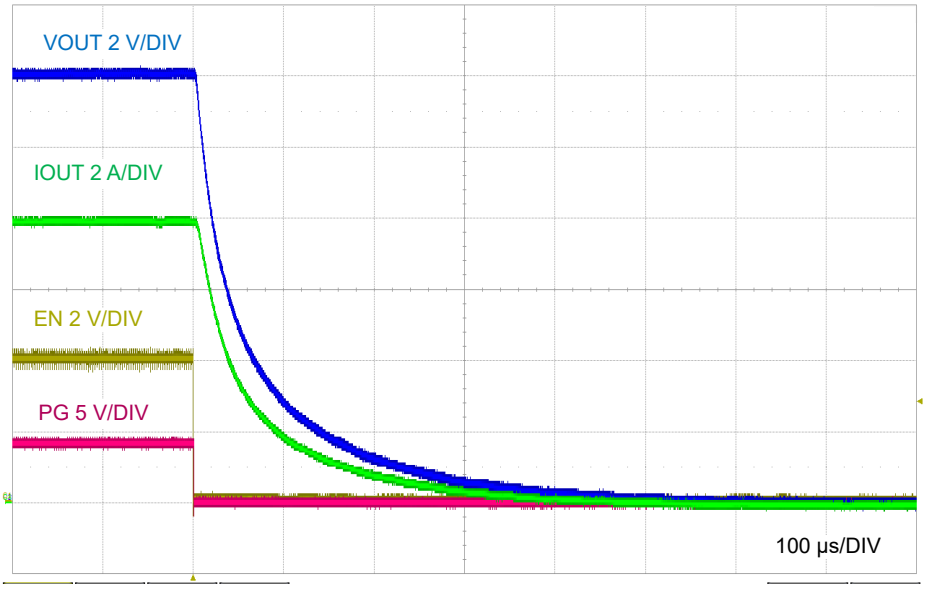


Figure 6-8. EN OFF, V_{IN} = 48 V, I_{OUT} = 8-A Resistive Load

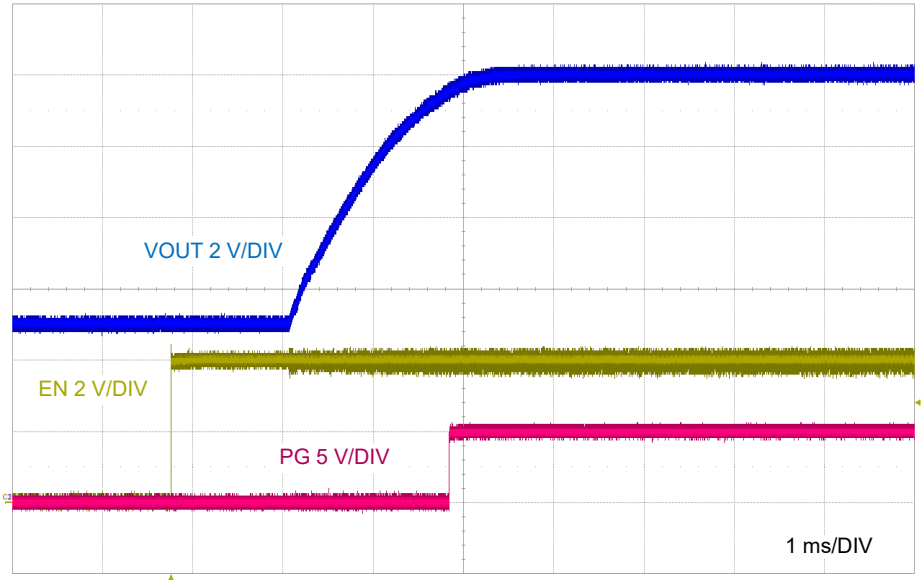


Figure 6-9. EN ON, V_{IN} = 48 V, V_{OUT} Prebiased at 5 V

6.2.5 Start-Up and Shutdown with VIN

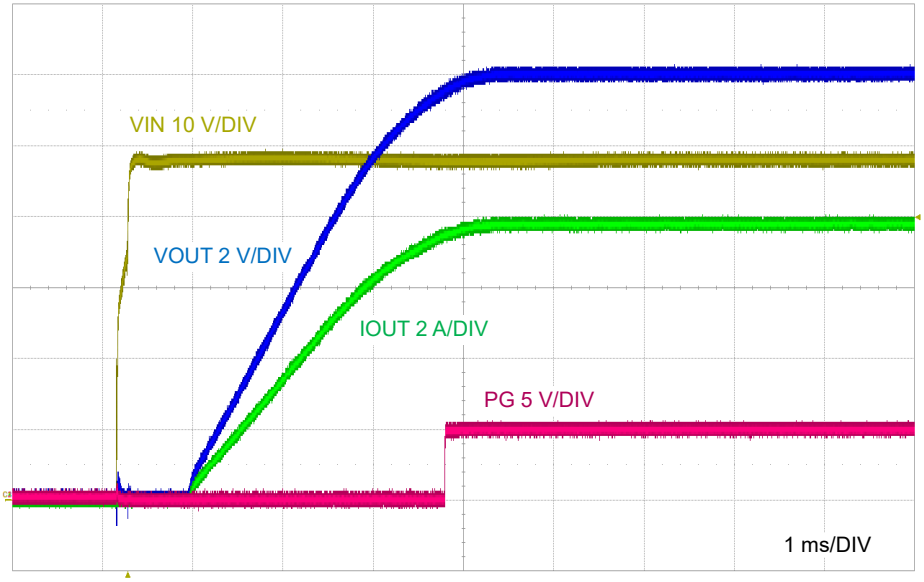


Figure 6-10. Start-Up, V_{IN} = 48 V, I_{OUT} = 8-A Resistive Load

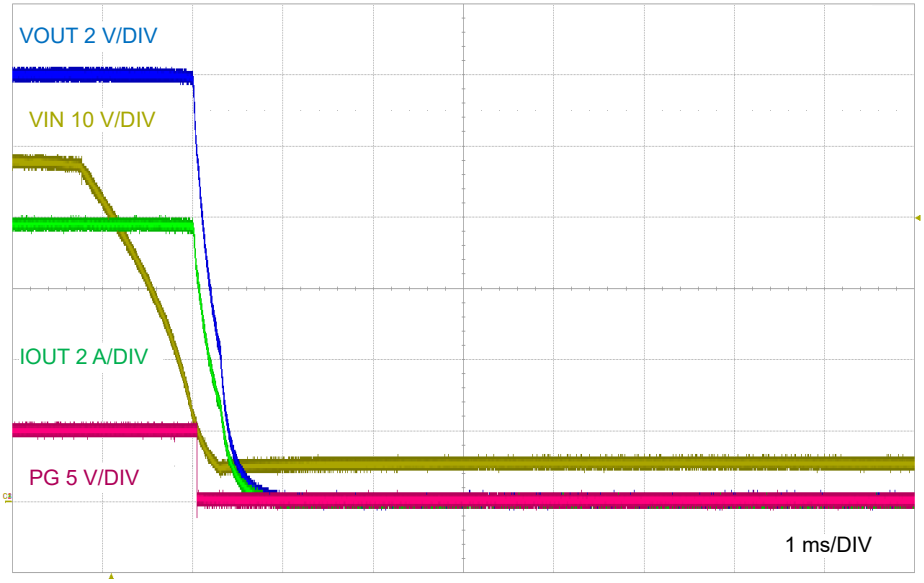
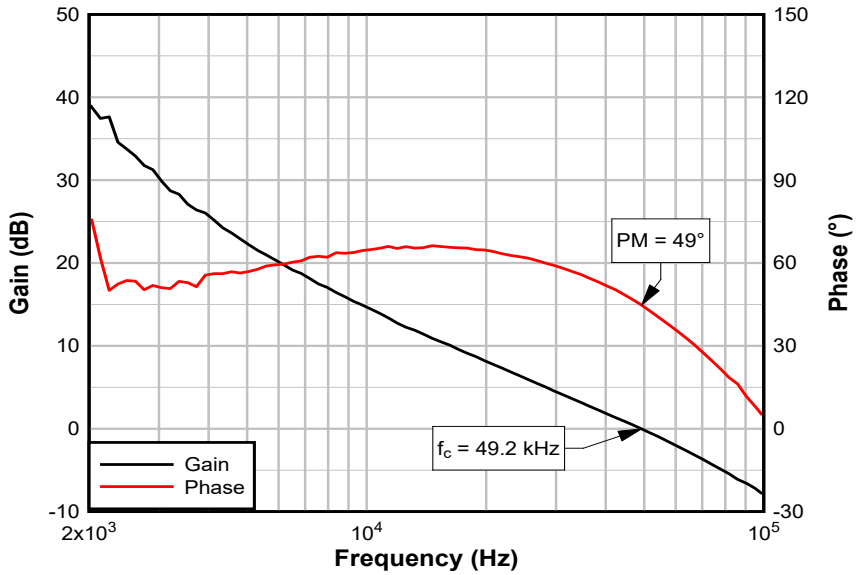


Figure 6-11. Shutdown, V_{IN} = 48 V, I_{OUT} = 8-A Resistive Load

6.3 Bode Plot



f_c = crossover frequency, PM = phase margin. Tested with R_{COMP} = 4.75 kΩ, C_{COMP} = 6.8 nF, and C_{HF} = 100 pF.

Figure 6-12. Bode Plot, V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 8-A Resistive Load

6.4 CISPR 25 EMI Performance

Figure 6-13 presents the EMI performance of the LM5149-Q1 EVM at 48-V input with Active EMI and DRSS mitigation techniques enabled. Conducted emissions are measured over a frequency range of 150 kHz to 30 MHz using a 5-µH LISN according to the CISPR 25 low-frequency specification. CISPR 25 Class 5 peak and average limit lines are denoted in red. The yellow and green spectra are measured using peak and average detection, respectively.

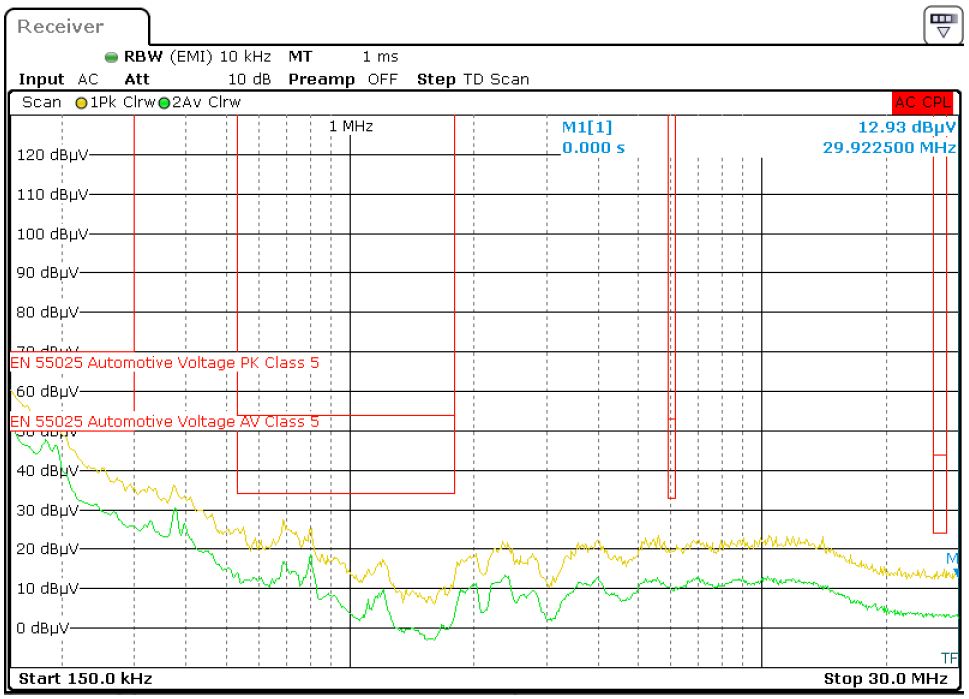


Figure 6-13. CISPR 25 Class 5 Conducted Emissions Plot, 150 kHz to 30 MHz, V_{IN} = 48 V, I_{OUT} = 5-A Resistive Load

6.5 Thermal Performance

Figure 6-14 shows the thermal performance image.

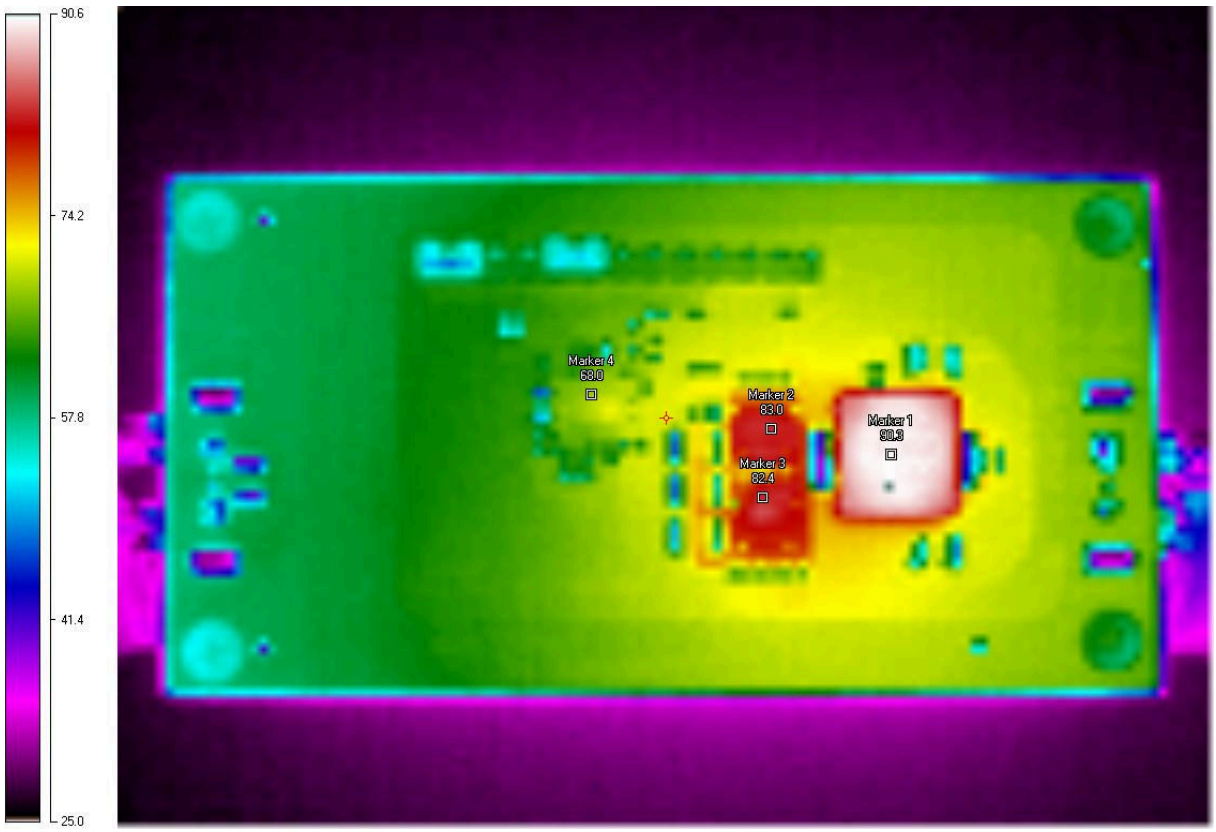


Figure 6-14. Thermal Performance, V_{IN} = 48 V, I_{OUT} = 8 A, T_{amb} = 25°C, No Airflow

7 EVM Documentation

7.1 Schematic

Figure 7-1 shows the EVM schematic.

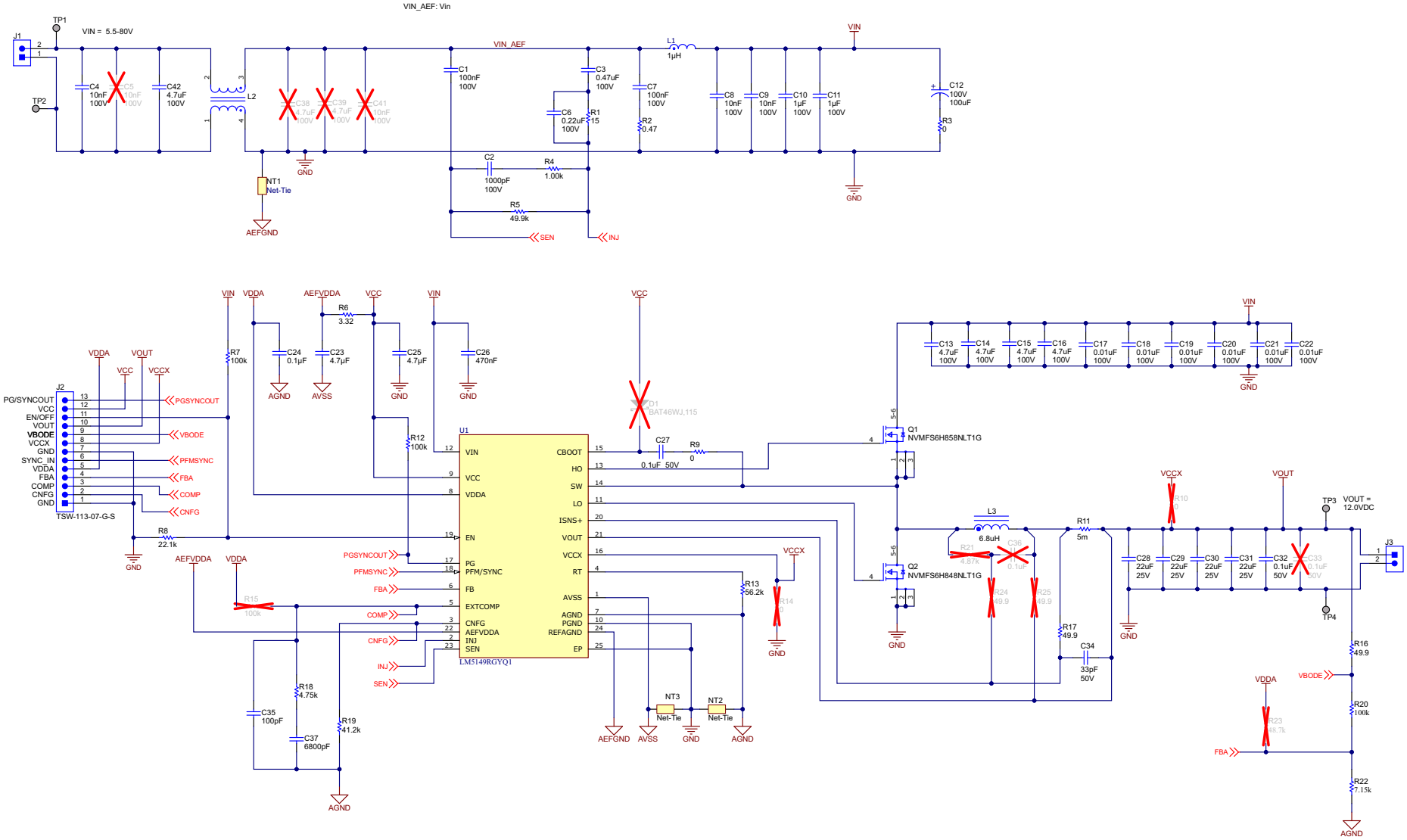


Figure 7-1. EVM Schematic

7.2 List of Materials

Table 7-1. List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
2	C1, C7	Capacitor, Ceramic, 0.1 µF, 100 V, X7R, 0603, AEC-Q200	GCJ188R72A104KA01D	Murata
1	C2	Capacitor, Ceramic, 1000 pF, 100 V, X7R, 0402, AEC-Q200	GRM155R72A102KA01D	Murata
1	C3	Capacitor, Ceramic, 0.47 µF, 100 V, X7R, 0805, AEC-Q200	CGA4J3X7S2A474K125AB	TDK
3	C4, C8, C9	Capacitor, Ceramic, 0.01 µF, 100 V, X7R, 0603, AEC-Q200	GCM188R72A103KA37J	Murata
1	C6	Capacitor, Ceramic, 0.22 µF, 100 V, X7R, 0603, AEC-Q200	HMK107C7224KAHTE	Taiyo Yuden
2	C10, C11	Capacitor, Ceramic, 1 µF, 100 V, X7R, 0805, AEC-Q200	08051C105K4Z2A	AVX
1	C12	Capacitor, Aluminum, 100 µF, 100 V, 0.33 Ω, AEC-Q200	EMVY101ARA101MKE0S	United Chemi-Con
5	C13, C14, C15, C16, C42	Capacitor, Ceramic, 4.7 µF, 100 V, X7S, 1210, AEC-Q200	CGA6M3X7S2A475K200AB	TDK
			GCM32DC72A475KE02L	Murata
6	C17, C18, C19, C20, C21, C22	Capacitor, Ceramic, 0.01 µF, 100 V, X7S, 0402 AEC-Q200	CGA2B3X7S2A103K050BB	TDK
1	C23	Capacitor, Ceramic, 4.7 µF, 25 V, X7R, 0805,AEC-Q200	CGA4J1X7R1E475K125AC	TDK
1	C24	Capacitor, Ceramic, 0.1 µF, 10 V, X7R, 0402, AEC-Q200	Std	Std
1	C25	Capacitor, Ceramic, 4.7 µF, 10 V, X7R, 0603	GRM188Z71A475ME15D	Murata
1	C26	Capacitor, Ceramic, 0.47 µF, 50 V, X7R, 0805 AEC-Q200	GCM21BR71H474KA55L	Murata
1	C27	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0402, AEC-Q200	CGA2B3X7R1H104K050BB	TDK
4	C28, C29, C30, C31	Capacitor, Ceramic, 22 µF, 25 V, X7R, 1210	GRM32ER71E226KE15L	Murata
1	C32	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	C0603C104K5RAC-TU	KEMET
1	C34	Capacitor, Ceramic, 33 pF, 50 V, C0G/NP0, 0402, AEC-Q200	GCM1555C1H330JA16D	Murata
1	C35	Capacitor, Ceramic, 100 pF, 50 V, C0G/NP0, 0402, AEC-Q200	CGA2B2C0G1H101J050BA	TDK
1	C37	Capacitor, Ceramic, 6800 pF, 50 V, X7R, 0402	GCM155R71H682KA55D	Murata
2	J1, J3	Terminal Block, 2 position, 5 mm, TH	Std	Std
1	J2	Header, 100 mil, 13 × 1, Au, TH	Std	Std
1	L1	Inductor, 1 µH, 8.2 mΩ typical, 6.3 A, 4 × 4 × 2.1 mm typ, AEC-Q200	XGL4020-102MEB	Coilcraft
1	L2	Common Mode Choke, 700 Ω at 100 MHz, 4 A, 15 mΩ, 7.0 × 6.0 × 3.8 mm typical, AEC-Q200	CM7060P701R-10	Laird
1	L3	Inductor, 6.8 µH, 12 mΩ, 13.3 A, 10.85 × 10 × 5.2 mm typical, AEC-Q200	VCHA105D-6R8MS6	Cyntec
		Inductor, 6.8 µH, 13.3 mΩ, 21.4 A, 10.5 × 10 × 6.5 mm typical, AEC-Q200	SPM10065VT-6R8M-D	TDK
1	Q1	MOSFET, N-Channel, 80 V, 19.5 mΩ, 12 nC, SON 5 × 6, AEC-Q101	NVMFS6H858NLT1G	Onsemi
1	Q2	MOSFET, N-Channel, 80 V, 8.8 mΩ, 25 nC, SON 5 × 6, AEC-Q101	NVMFS6H848NLT1G	Onsemi
1	R1	Resistor, Chip, 15 Ω, 1/16 W, 1%, 0402	Std	Std
1	R2	Resistor, Chip, 0.47 Ω, 1/10 W, 5%, 0603	Std	Std
1	R3	Resistor, Chip, 0 Ω, 1/8 W, 1%, 0805	Std	Std
1	R4	Resistor, Chip, 1 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R5	Resistor, Chip, 49.9 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R6	Resistor, Chip, 3.32 Ω, 1/16 W, 1%, 0402	Std	Std
1	R7	Resistor, Chip, 100 kΩ, 1/10 W, 1%, 0603	Std	Std
1	R8	Resistor, Chip, 22.1 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R9	Resistor, Chip, 0 Ω, 1/5 W, 1%, 0402	Std	Std
1	R11	Resistor, Chip, 5 mΩ, 1 W, 1%, 0508, AEC-Q200	KRL2012E-M-R005-F-T5	Susumu
2	R12, R20	Resistor, Chip, 100 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R13	Resistor, Chip, 56.2 kΩ, 1/16 W, 1%, 0402	Std	Std
2	R16, R17	Resistor, Chip, 49.9 Ω, 1/16 W, 1%, 0402	Std	Std
1	R18	Resistor, Chip, 4.75 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R19	Resistor, Chip, 41.2 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R22	Resistor, Chip, 7.15 kΩ, 1/16 W, 1%, 0402	Std	Std
4	TP1, TP2, TP3, TP4	Test Point, Miniature, SMT	5019	Keystone
1	U1	IC, LM5149-Q1, 80-V Synchronous Buck Controller, VQFN-24	LM5149QRGYRQ1	TI
1	PCB1	PCB, FR4, 6 layer, 2 oz, 83 mm × 43 mm	PCB	–

7.3 PCB Layout

Figure 7-2 through Figure 7-9 show the design of the LM5149-Q1 EVM using a six-layer PCB with 2-oz copper thickness. The power stage is essentially a single-sided design and the input filtering is located on the bottom side.

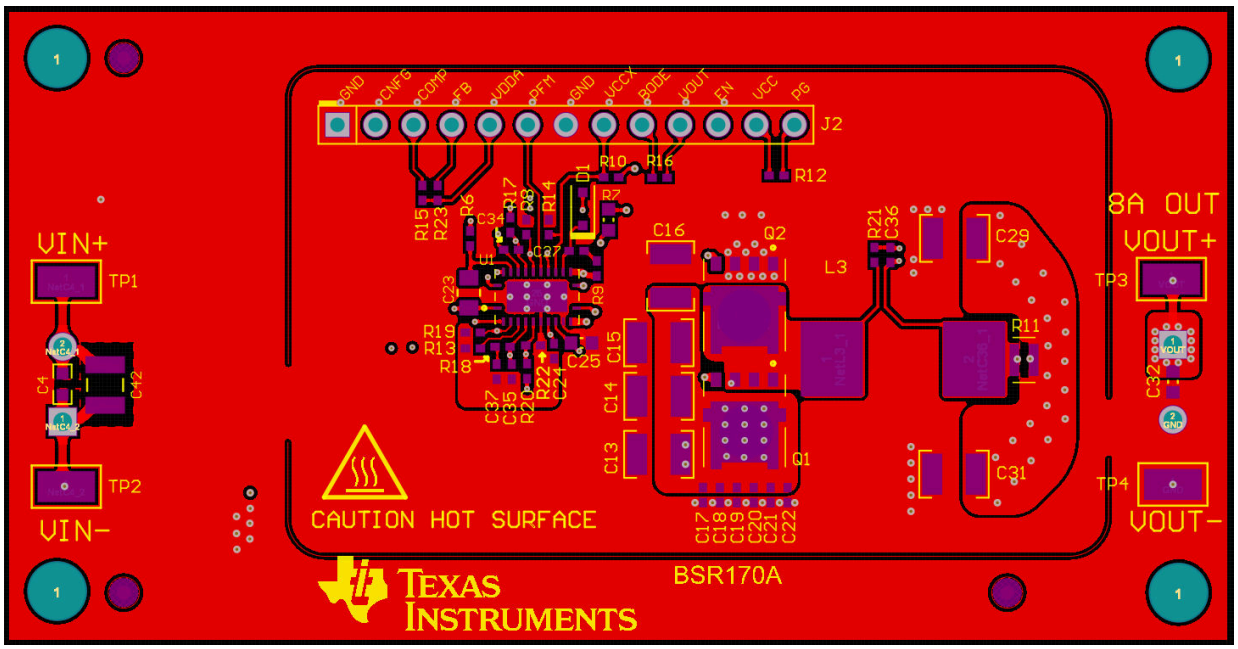


Figure 7-2. Top Copper (Top View)

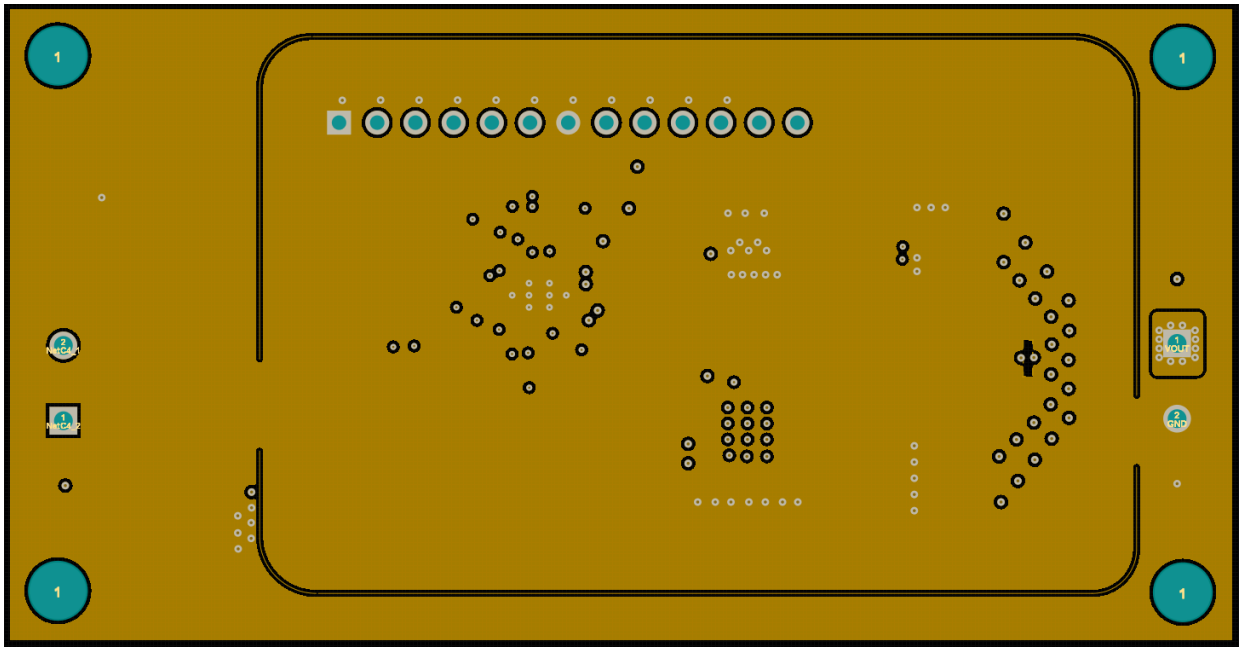


Figure 7-3. Layer 2 Copper (Top View)

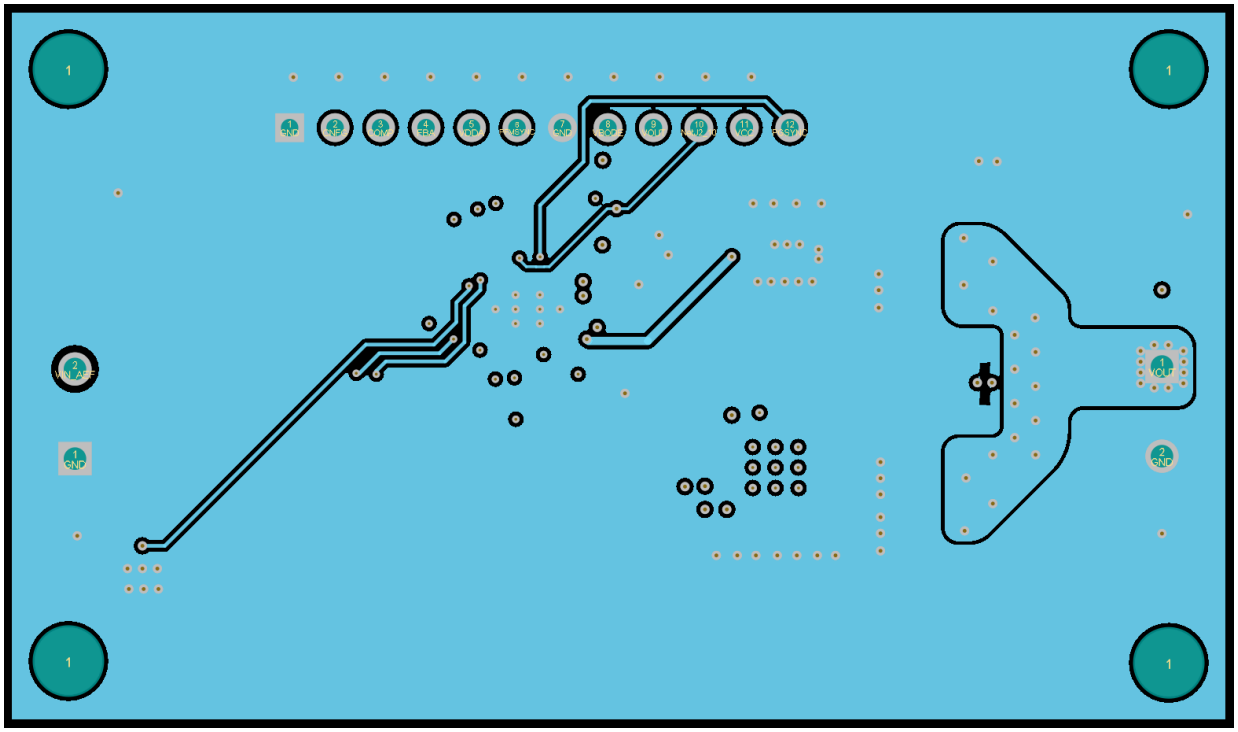


Figure 7-4. Layer 3 Copper (Top View)

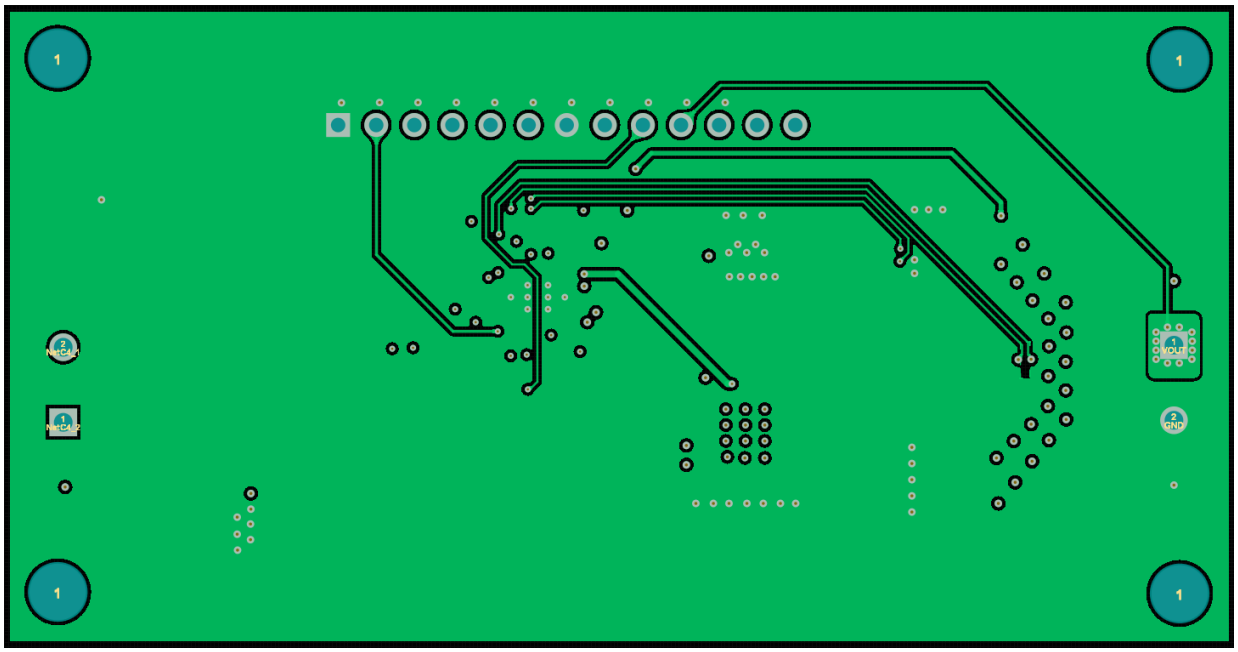


Figure 7-5. Layer 4 Copper (Top View)

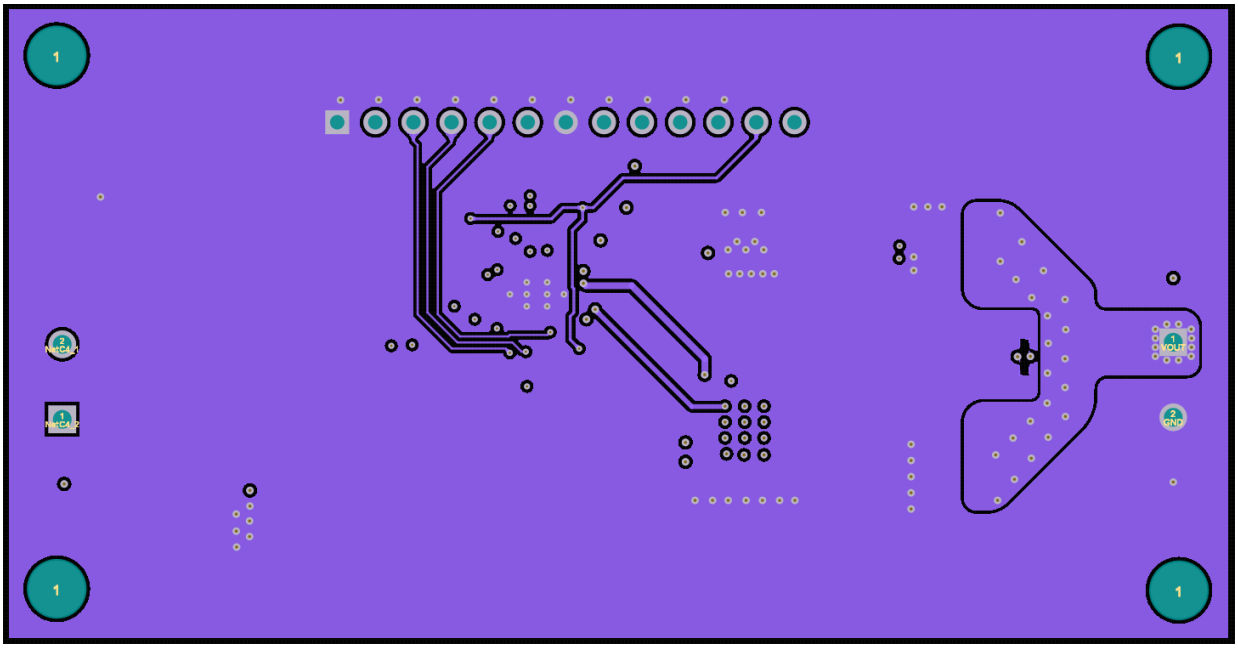


Figure 7-6. Layer 5 Copper (Top View)

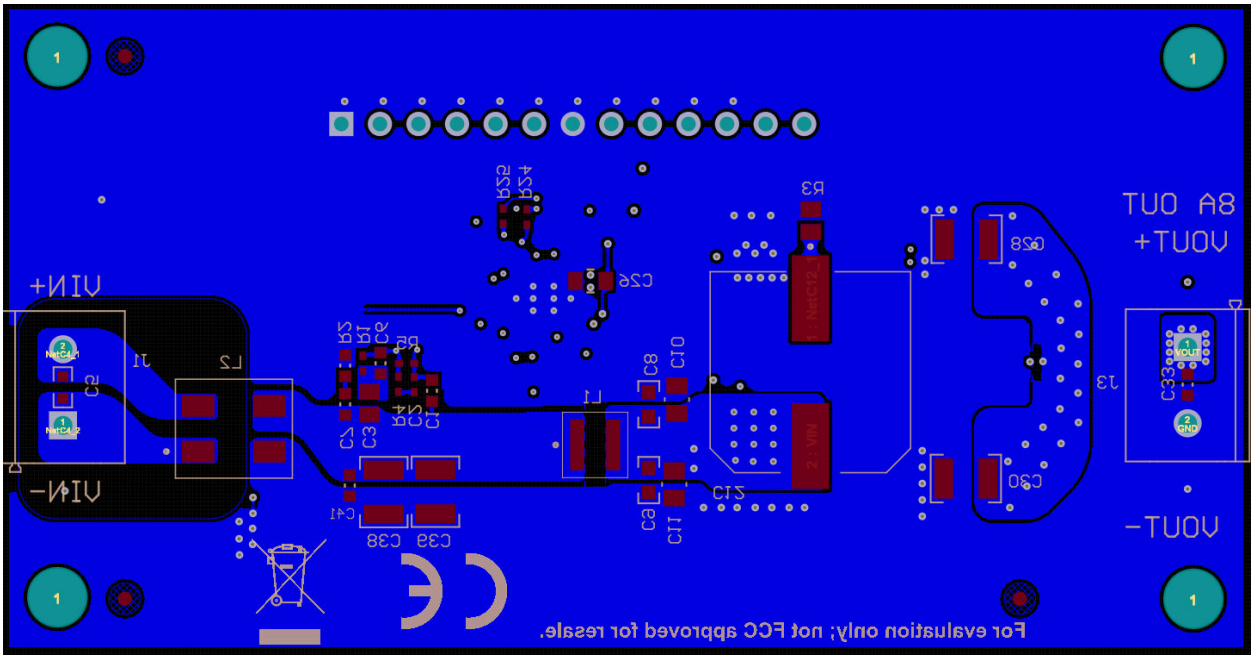


Figure 7-7. Bottom Copper (Top View)

7.4 Component Drawings

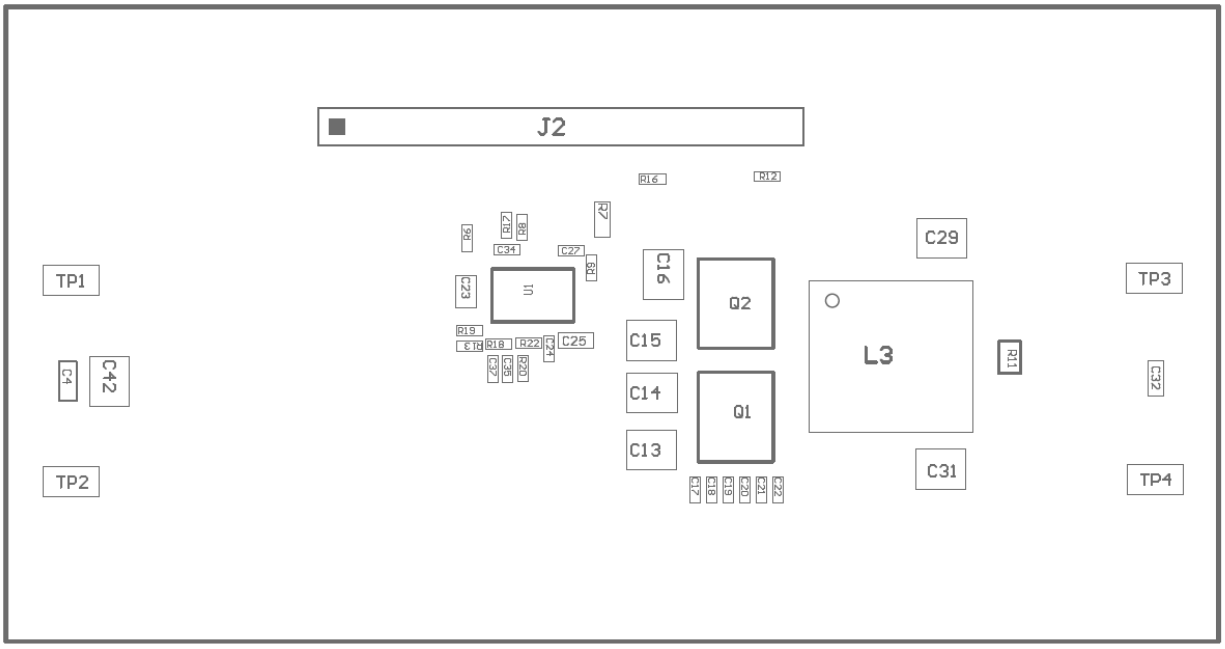


Figure 7-8. Top Component Drawing

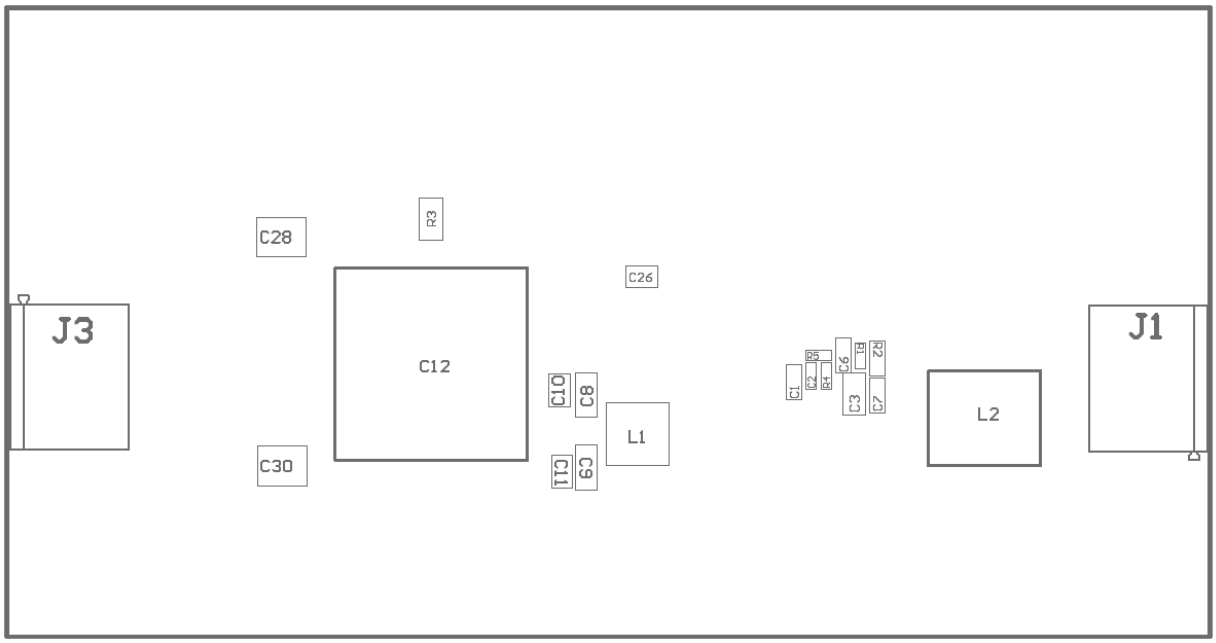


Figure 7-9. Bottom Component Drawing

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For development support see the following:

- For TI's reference design library, visit TI reference designs
- For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
- LM5149-Q1 DC/DC Controller Quickstart Calculator

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *LM5149-Q1 3.5-V to 80-V Synchronous Buck DC/DC Controller Data Sheet*
- *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout Application Brief*
- *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics Analog Applications Journal*
- *AN-2162 Simple Success with Conducted EMI from DC-DC Converters Application Report*
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*

8.2.1.1 PCB Layout Resources

- *AN-1149 Layout Guidelines for Switching Power Supplies Application Report*
- *AN-1229 Simple Switcher PCB Layout Guidelines Application Report*
- *Constructing Your Power Supply – Layout Considerations Power Supply Design Seminar*
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x Application Report*
- Power House Blogs:
  - *High-Density PCB Layout of DC-DC Converters*

8.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design by Insight, Not Hindsight Application Report*
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD Thermally Enhanced Package Application Report*
- *PowerPAD Made Easy Application Brief*
- *Using New Thermal Metrics Application Report*

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