TMS320DM642 to TMS32DM6467 Migration

DSPS Applications

ABSTRACT

This document describes device considerations to migrate a design based on a TI TMS320DM642 video/imaging fixed-point Digital Signal Processor (DSP) to one based on a TI TMS320DM6467 Digital Media System-on-Chip (DMSoC). These two devices are based on similar DSP CPU cores, feature video processing capability, and a mixture of memory and other peripherals useful in a system environment. This document describes the details for performing this migration.

Since this document describes migration from a TMS320DM642 device to a TMS320DM6467 device, familiarity with the TMS320DM642 device and its documentation is assumed.

Note that all of the documentation referenced in this migration guide can be found on the TI website located in the two device respective product folders. The device folders are found at the following web pages.

- TMS320DM642 - http://focus.ti.com/docs/prod/folders/print/tms320dm642.html
- TMS320DM6467 - http://focus.ti.com/docs/prod/folders/print/tms320dm6467.html

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1 Basic Feature Comparison

Table 1 shows a comparison of the basic features of the TMS320DM642 and the TMS320DM6467. The remainder of this document presents a comparison of these features in greater detail, and also provides references to the appropriate documentation for further information.

Table 1. DM642/DM6467 Basic Feature Comparison

HARDWARE FEATURES				DM642	DM6467
CPU	DSP			C64x	C64x+
	ARM			-	ARM926EJ-S
Speeds	DSP			500/600/720 MHz	594-/729 MHz
	ARM			-	297/364.5 MHz
Endianness				Little/Big	Little
Memory	DSP	Cache: L1P		16 K-Byte	32 K-Byte
		Cache: L1D		16 K-Byte	32 K-Byte
		Cache: L2		256 K-Byte	128 K-Byte
	ARM	Data/Program RAM		-	32 K-Byte
		Data/Program ROM		-	8 K-Byte
		Instruction Cache		-	16 K-Byte
		Data Cache		-	8 K-Byte
Peripherals		VCXO Interpolated Control Port		1	-
		Video/Imaging Coprocessor		-	2 HDVICP
		Video Port Interface (VPIF)		3	1
		Video Data Conversion Engine (VDCE)		-	1
		DDR2 EMIF		-	1
		Asynchronous EMIF (EMIFA)		1	1
		EDMA	EDMA Controller	1	1
			Transfer Controller	1	4
		Transfer Controller		1	1
		PCI		1	1
		Timers		3, 32-bit	2, 64-bit
		Watchdog Timer		-	1
		UART		-	3
		SPI		-	1

Table 1. DM642/DM6467 Basic Feature Comparison (continued)

HARDWARE FEATURES		DM642	DM6467
	PLL	1	2
	I2C	1	1
	Serial Ports	McASP, 2 McBSP	2 McASP
	EMAC	10/100 EMAC	10/100/1000 EMAC
	USB 2.0	-	1
	VLYNQ	-	1
	HPI	1 16-/32-bit	1 16-/32-bit
	GPIO	Up to 16 pins	Up to 33 pins
	PWM	-	2 outputs
	ATA/ATAPI I/F	-	1
	PCI	1 32-bit, 66 MHz	1 32-bit, 33 MHz
	MDIO	1	1
	Clock Recovery Generator	-	1
Voltage	Core (V)	1.2 V (500), 1.4 V (all)	1.2 V
	I/O (V)	3.3 V	1.8 V, 3.3 V
Packages		548-pin BGA	529-pin BGA

2 CPU Core Considerations

The DM6467 device contains an ARM CPU as well as a DSP CPU core. The DM642 device contains only a DSP CPU core. The following sections discuss considerations of the different CPU cores provided on these two devices.

2.1 DSP CPU Core Considerations

The TMS320DM642 and TMS320DM6467 devices utilize a TMS320C64x™ DSP CPU core; therefore, they offer similar features and architecture. However, the DM6467 utilizes an enhanced version of the DSP CPU core, designated the TMS320C64x+™, which implements numerous additional features not found in the earlier DSP CPU. Accordingly, the DM6467 offers capabilities beyond those found on the DM642. In particular, the C64x+™ DSP architecture adds several new instructions and features giving you improved performance for operations used in video applications and other general purpose algorithms. The C64x+ DSP core is based on the C64x™ DSP core, and most C64x software executes properly on the C64x+ after being recompiled for the enhanced core and after being adjusted for memory map differences.

Note that differences between the two CPUs exist in the following areas that may affect existing code:

- Instruction Set
- Registers
- Interrupts
- DMA Operations
- Timing Changes
- Circular Addressing

The following are among the new enhancements added to the C64x+ DSP core CPU in order to realize performance improvements on this new architecture:

- New instructions to support increased code efficiency and speed
- New 16-bit compact instructions to support increased code density
- New SPLOOP facility to provide improved code compactness and interruptibility for pipelined loops
- Changes to internal memory to increase the flexibility of internal memory usage

- New privilege modes to support secure operating systems
- New support for exceptions to provide improved error handling capabilities

For detailed information regarding the difference between the C64x and C64x+ DSP core, see the *TMS320C64x to TMS320C64x+ CPU Migration Guide* (SPRAA84). For additional information, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732).

ARM CPU Core Considerations

The DM6467 features the ARM subsystem designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device, including the DSP subsystem, the video processing subsystem (VPSS), and a majority of the peripherals and external memories.

In the DMSoC, the ARM handles system functions such as system-level initialization, configuration, user interface, user command execution, connectivity functions, interface and control of the DSP subsystem, and overall system control. The ARM performs these functions because it has a larger program memory space and better context switching capability, and is more suitable for complex multi-tasking and general-purpose control tasks than the DSP.

The ARM9 processor supports the 32-bit ARM and 16-bit THUMB instruction sets, enabling you to trade off between high-performance and high code density. The processor also supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM9 processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The processor has Harvard architecture and provides a complete high-performance subsystem, including:

- ARM926EJ-S integer core
- CP15 system control coprocessor
- Memory Management Unit (MMU)
- Separate instruction and data Caches
- Write Buffer
- Separate instruction and data tightly-coupled memories (TCMs) [internal RAM] interfaces
- Separate instruction and data AHB bus interfaces
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)

For more detailed information about the ARM processor core, see the *ARM926EJ-S Technical Reference Manual*, available at: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0198e/index.html.

CPU Clock Speeds

The DM642 and DM6467 both offer a variety of different speed versions to accommodate a range of different performance requirements.

Table 2 shows a summary of the different speed versions of the DM642 and DM6467.

Table 2. Available Performance Versions of the DM642 and DM6467

	DM642	DM6467
DSP CPU	500 MHz (2.00 ns cycle time) 600 MHz (1.67 ns cycle time) 720 MHz (1.39 ns cycle time) (1)	594 MHz (1.68 ns cycle time) 729 MHz (1.37 ns cycle time)
ARM CPU	-	297 MHz (3.37 ns (cycle time) 364.5 MHz (2.74 ns cycle time)

(1) Commercial temperature range only

Note that power supply voltage requirements are different on these devices for some of the different speed versions. See Section 10 of this document for detailed information regarding power supply voltage requirements for the DM642 and DM6467.

For additional detailed information regarding performance, timing requirements, and characteristics for the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

2.2 Endianness Considerations

The DM642 is capable of functioning in either big-endian or little-endian operating mode. On the other hand, the DM6467 functions only in little-endian operating mode. Accordingly, software running in big-endian mode on the DM642 that is to be ported to the DM6467 frequently needs to be modified and recompiled in little-endian mode. Also, some peripheral modules have their own unique endianness considerations; therefore, for each peripheral used in a DM6467 application, the peripheral user's guide should be consulted for specific endianness considerations.

3 Internal Memory Comparisons

The DM642 and DM6467 feature on-chip internal memories, allowing efficient handling of varied partitions of internal program and data information. The devices feature several different types of cache memory, allowing significant flexibility in using memory to enhance algorithm performance. The DM6467 also provides an on-chip ROM, which contains the boot-loader program. Since there are some differences between the memory architectures on the two devices, some software modifications are required when migrating an application from the DM642 to the DM6467.

The DM6467 contains ARM and DSP CPU cores and memory usage is partitioned between the two CPUs; therefore, certain areas of internal memory, although accessible to both CPUs, are typically used more by one CPU than the other.

3.1 DSP Internal Memory Comparison

The DM642 uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 128K-bit direct mapped cache and the Level 1 data cache (LID) is a 128K-bit 2-way set associative cache. The Level 2 memory/cache (L2) consists of a 2M-bit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two.

The DM6467 C64x+ core also uses a two level cache-based architecture. The Level 1 program memory/cache consists of 32 KB memory space that can be configured as mapped memory or direct mapped cache. The Level 1 data memory/cache consists of 32 KB that can be configured as mapped memory or 2-way set associative cache. The Level 2 memory/cache consists of a 128 KB RAM memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both. Table 3 shows a comparison of the DM642 and DM6467 DSP internal memory.

Table 3. DSP Internal Memory Comparison

Memory Type	DM642	DM6467
L1P Program Memory	16 K-bytes cache (direct mapped)	32K-bytes RAM/Cache (mapped memory or direct mapped cache)
L1D Data Memory	16 K-bytes cache (2-way set associative)	32K-bytes RAM/Cache (mapped memory or 2-way set associative cache)
L2 RAM Memory	256 K-bytes unified mapped RAM/Cache (4-way set associative), flexible allocation	128K-bytes unified mapped RAM/Cache

For additional detailed information regarding the use of the DM6467's internal memory, see the *TMS320C64x+ DSP Cache User's Guide* (SPRU862).

3.2 DM6467 ARM Internal Memory

The DM6467 ARM has access to 8 K-bytes ARM Internal ROM that can be used for instructions or data. The TMS320DM6467 includes 32 K-bytes ARM internal RAM logically separated into 16K-byte pages. The device also contains 16K-bytes instruction Cache and 8K-bytes of data Cache used by the CPU to enhance instruction and data handling. Table 4 shows the DM6467 ARM internal memory configuration.

Table 4. DM6467 ARM Internal Memory

Memory Type	DM6467
Data/Program RAM	32 K-bytes
Data/Program ROM	8 K-bytes
Program Cache	16 K-bytes
Data Cache	8 K-bytes

For additional detailed information regarding use of the DM6467 internal memory, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403) and the *TMS320646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

4 Peripherals

The TMS320DM642 and TMS320DM6467 both feature a wide variety of peripheral modules that are useful in many different system environments. This section presents a comparison of the peripheral offerings on these two devices.

4.1 Video Ports

The DM642 and DM6467 feature video processing peripherals that can accept video input and generate video output. The DM642 has three configurable video ports, each of which can be programmed for either video input or video output. The DM642 also features a VCXO interpolated control (VIC) port. The DM6467 uses the video data conversion engine (VDCE) and video port interface (VPIF) with two input channels and two output channels. The DM6467 also features a high definition (HD) video/imaging co-processor; therefore, each device can accept a video input stream and generate a video output stream.

4.1.1 Video Port Interface Comparisons

The DM642 video port peripheral can operate as a video capture port, video display port, or transport stream interface (TSIF) capture port. The device contains three configurable video ports, each with two channels: A and B. The entire port (both channels) is always configured for either video capture or display only. For video capture operation, the DM642 video port can operate as two 8/10-bit channels of BT.656 or raw video capture; or as a single channel of 8/10-bit BT.656, 8/10 bit raw video, 16/20-bit Y/C video, 16/20-bit raw video, or 8-bit TSI. For video display operation, the DM642 video port can operate as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20 bit Y/C video, or 16/20-bit raw video. It can also operate in a two channel 8/10-bit raw mode in which the two channels are locked to the same timing. Channel B is not used during single operation.

The DM6467 VPIF has two input channels that receive video byte stream data and two output channels that video byte stream data is asserted, all channels can be activated simultaneously. Channels 0 and 1 are prepared only for input. The following configurations are allowed for the input channels: two 8-bit standard definition video with embedded timing codes (BT.656), or one single 16-bit HD video with embedded timing codes (BT.120), or a single raw video (8-/10-/12-bit). Channels 2 and 3 are prepared only for output. The following configurations are allowed for the output channels: two 8-bit standard video display channels with embedded timing codes or one single 16-bit HD video display with embedded timing codes.

The DM6467 VPIF capture channel input data format is selectable based on the settings of the specific Channel Control Register, Channels0-3. Both NTSC and PAL formats are supported for this device. VBI is not supported for ITU-BT.1120 (HDTV). VBI is necessary only for ITU-BT.656 (SDTV); in this case, VBI format has to be based on ITU-BT.1364. Table 6 describes the usage combinations that are supported in the DM6467 VPIF.

Table 5. DM6467 VPIF Supported Video Formats

Input	Supported Formats	
TV System Format	HDTV(rec.1120)	SDTV (rec. 656)
NTSC	1125 line/60 field (vertical) 2200 pixel (horizontal)	525 line/60 field (vertical) 858 pixel (horizontal)
PAL	1250 line/50 field (vertical) 2304 pixel (horizontal)	625 line/50 field (vertical) 864 pixel (horizontal)
Square pixel common image format	1080-30p	-

Table 6. Input and Output Usage Combinations on the DM6467 VPIF

Input Format	DM6467		
	HDTV Output	SDTV Output	No Output
HDTV Input (1 channel only)	X	X	X
Raw Capture Mode	X	X	X
SDTV Input	X (both 1-channel and 2-channel input)	X (both 1-channel and 2-channel input/output)	X (both 1-channel and 2-channel input)
No Input	X	X(both 1-channel and 2-channel output)	

In the DM6467 VPIF, both the input data and output data are stored in SDRAM. All video data is divided into image data and VBI data. The image data is divided into luminance and chrominance data in each field independently. Each start address in SDRAM can be configured by the ARM processor through the register interface.

For more detailed information regarding the use of the DM6467 VPIF, see the *TMS320646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

4.1.2 VCXO Interpolated Control Port

The DM642 VIC port provides digital-to-analog conversion with resolution from 9 bits to up to 16 bits. The output of the VIC is a single bit interpolated D/A output (VDAC pin). The DM6467 does not feature a dedicated VIC port; however, this function can be implemented in a DM6467 system using a pulse width modulator (PWM) output and a timer input.

4.1.3 Video Data Conversion Engine

The DM6467 features a VDCE used for video data processing. The VDCE has several capabilities of not only pure video data processing but also functions that are required from a video codec module.

The VDCE supports a down-scaler function on horizontal (HRSZ) and vertical (VRSZ) with ratio defined by 256/N (N is natural number that ranges from 256 to 2048) with 4 taps interpolation. Magnification ratio of horizontal and vertical down-scaler can be configured separately.

The horizontal down-scaler module has an anti-alias filter (7 taps) for luminance data, pixel interpolation (4 taps) for common use of luminance and chrominance data, and size clipping to configure size on the module register. The method of vertical down-scaler varies from picture format, interlace, or progressive. In interlace format, the vertical down-scaler function performs for each field independently. All source pixels of interpolation are derived by the same field.

The VDCE also features a chrominance conversion module used for format conversion of chrominance signal between 4:2:2 and 4:2:0 formats. The 4:2:0 format is mainly used for video codec and the 4:2:2 format is mainly used for input or output video signals such as BT.656 or BT.1120.

The VDCE does not have multiple video window/on-screen display (OSD) window support. The VDCE features a 2-bit hardware menu overlay function that can blend video image and artificial bitmap data (2 bits/pixel), like a light OSD function. The 2-bit hardware menu overlay function reads two kinds of data (video and bitmap) from SDRAM, and overlays them to one display output data with blending.

The VDCE also features edge padding for enhancement of reference image data to be used in motion compensation function with unrestricted motion vector that is defined in specification H.264, VC-1, and MPEG-4. This module copies all edge pixels to the external side of the reference data with configured width for both horizontal and vertical directions (both upper and lower, both left and right of the image data). The method of edge padding varies in two ways: progressive format and interlaced format.

For detailed information regarding the use of the VDCE, see the *TMS320DM646x DMSoC Video Data Conversion Engine (VDCE) User's Guide* (SPRUEQ9).

4.2 External Memory Interface (EMIF)

The DM642 and DM6467 feature flexible external interfaces that support accessing various types of memory devices. The specific external memory interfaces used by the two devices are implemented differently. A single 64-bit external memory interface is used for all types of memory supported on the DM642. Two separate external memory interfaces are used on the DM6467: one dedicated to DDR2 memory and a second interface for asynchronous memories.

Therefore, when architecting an external memory interface for a DM6467 system, a different approach is generally used than with the DM642. Instead of having only one external memory interface for all devices, the DM6467 can partition accesses on two separate memory interfaces, allowing for improved efficiency and throughput.

The DM6467 DDR2 interface utilizes a 16- or 32-bit data bus, and is optimized for use with high-speed, high-density DDR2 memory storage of programs and large blocks of data. Master peripherals, enhanced direct memory access (EDMA), the ARM processor, and DSP can access the DDR2 memory controller through the switched central resource (SCR). Table 7 summarizes the characteristics of the DM642 and DM6467 external memory interfaces.

For detailed information regarding the use of the DM6467 DDR2 memory interface, see the *TMS320DM646x DMSoC DDR2 Memory Controller User's Guide* (SPRUEQ4).

Table 7. DSP Internal Memory Comparison

Features	DM642	DM6467
Data Width	64 bits	16-/32- bits
• Memory Types	Sync/Async	DDR2
• Address Range	1024 Mbytes	256 Mbytes
Data Width	NA	8-/16-bits
• Memory Types	NA	Async
• Address Range	NA	

The asynchronous memory interface provides a means to connect to slower special purpose memory including; NAND flash, asynchronous devices including flash and SRAM, and host processor interfaces such as the host port interface (HPI). The DM6467 supports 4 addressable chip select spaces of up to 32MB each, with 8-bit and 16-bit data bus widths. The EMIF pins are multiplexed with other peripherals such as PCI, HPI, GPIO, and ATA.

For detailed information regarding the use of the DM6467 EMIFA, see the *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (SPRUEQ7).

4.3 Enhanced Direct Memory Access (EDMA) Controllers

The DM642 and DM6467 feature EDMA controllers that can be used to transfer data to and from numerous locations, both on- and off-chip. Both devices support 64 independent channels of EDMA transfers.

The DMA controllers used on these two devices are functionally similar; however, the DM642 uses version 2.0 of the EDMA controller, and the DM6467 uses version 3.0 of the EDMA controller. Migration from EDMA 2.0 to EDMA 3.0 is discussed in detail in the *EDMA v3.0 (EDMA3) Migration Guide for TMS320DM644x DMSoC* (SPRAAA6).

The DM6467 EDMA controller has a RAM-based architecture. The parameter RAM (PaRAM) table is segmented into multiple PaRAM sets, each including eight 4-byte PaRAM set entries that includes typical DMA transfer parameters such as source address, destination address, transfer counts, indexes, options, etc. There are 512 PaRAM sets in the DM6467 EMDA controller.

The DM6467 provides four EDMA queues and four transfer controllers. The DM6467 offers six transfer completion interrupts and five error interrupts. Table 8 shows the features of the DM6467 EDMA.

Table 8. DM6467 EDMA Features

Features	TC	DM6467
Number of PaRAM Sets		512
Number of Queues		4
Number of Transfer Controllers		4
Default Burst Size	TC0	
	TC1	Fixed – 32 bytes
	TC2	Fixed – 32 bytes
	TC3	Fixed – 32 bytes
Transfer Completion Interrupts		6 (Shadow Region 0,1,4,5,6,7)
Error Inturrupts		5 (Globa l+ TC0+TC1 +TC2 +TC3)

For detailed information regarding the use of EDMA on the DM6467, see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUEQ5).

4.4 Peripheral Component Interconnect (PCI) Interface

The DM642 and DM6467 feature an integrated peripheral that is compatible with the industry standard peripheral component interconnect (PCI) interface. The PCI interfaces on these two devices are similar in function and pinout; however, the DM642 PCI interface complies with version 2.2 of the PCI specification and the DM6467 PCI complies with version 2.3 of the PCI specification. Also, the DM642 PCI runs at a maximum of 66 MHz and the DM6467 PCI runs at a maximum of 33 MHz. Accordingly, use of these two peripherals is different, therefore, migrating an application from a DM642 to a DM6467 requires software and hardware interconnection changes.

For detailed information regarding the use of the PCI interface on the DM6467, see the *TMS320DM646x DMSoC Peripheral Component Interconnect (PCI) User's Guide* (SPRUER2).

4.5 Serial Ports

The DM642 and the DM6467 feature serial port interfaces to provide connectivity to a wide variety of external devices including codecs, communications peripherals, and other processors. The DM642 features one multi-channel audio serial port (McASP) and two multi-channel buffered serial ports (McBSP), and the DM6467 features two McASPs. Information on these peripheral modules is presented in the following sections.

4.5.1 McBSP Serial Port

The DM642 features a McBSP peripheral module, while the DM6467 does not; therefore, DM642 applications utilizing the McBSP requires some modifications when migrating between these two devices.

4.5.2 McASP Serial Port

The DM642 and DM6467 feature a general-purpose audio serial port optimized for the needs of multichannel audio applications. This peripheral module is useful for time-division multiplexed (TDM) streams, inter-integrated sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

The DM642 includes one McASP interface peripheral (McASP0). This module consists of transmit and receive sections that can operate synchronized or completely independently with separate master clocks, bit clocks, and frame syncs, using different transmit modes with different bit-stream formats. The DM642 McASP module also includes up to 16 serializers that can be individually enabled to either transmit or receive. In addition, all of the DM642 McASP pins can be configured as general-purpose input/output (GPIO) pins.

The DM6467 has two instances of the McASP. The McASP0 module includes up to four serializers that can be individually enabled to either transmit or receive in all different modes. The McASP 1 module is limited with only one pinned-out serializer that can be enabled to only transmit in DIT mode (neither receiving in any mode nor transmitting in either burst or TDM mode is supported). The GPIO functionality internal to the McASP is also not supported.

Other differences in usage between these devices include the base addresses of the memory mapped registers, signal locations within the device pinouts, and pin multiplexing selection.

For detailed information regarding the use of the McASP on the DM6467, see the *TMS320DM646x DMSoC Multichannel Audio Serial Port (McASP) User's Guide* (SPRUER1).

4.6 Serial Peripheral Interface (SPI) Port

The DM6467 features a dedicated serial peripheral interface (SPI) port that allows a serial bit stream of programmed length to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications include an interface to external input/output (I/O) or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMS and analog-to-digital converters (ADC).

The module allows serial communications with other SPI devices through a 3-pin, 4-pin, or 5-pin mode interface. Table 9 shows the DM6467 SPI pins used to interface to external devices.

Table 9. DM6467 SPI Pins

Pin	DM6467 Type [1]	Function
SPI_CLK	I/O	Serial clock input in slave mode, serial clock output in master mode
SPI_SIMO	I/O	Serial data input in slave mode, serial data output in master mode
SPI_SOMI	I/O	Serial data output in slave mode, serial data input in master mode
$\overline{\text{SPI\_CS0}}$	I/O	Slave 0 chip select output in master mode, input in slave mode
$\overline{\text{SPI\_CS1}}$	I/O	Slave 1 chip select output in master mode, input in slave mode
$\overline{\text{SPI\_EN}}$	I/O	Input in master mode, output in slave mode indicating slave is ready to be served

(1) I = Input, O = Output

The device supports multi-chip select operation for up to two SPI slave devices. The SPI on the DM6467 operates as both a master and a slave device. The MASTER and CLKMOD bits in the SPI Global Control Register 1 (SPIGCR1) must be set to 1 for SPI to function as a master and cleared to 0 for SPI to function as a slave.

Table 10. DM6467 SPI Feature Comparison

Feature	DM6467
Operation Mode	Master/Slave
Chip Selects	$\overline{\text{SPI\_CS0}}$, $\overline{\text{SPI\_CS1}}$
Wire Interface	3-pin, 4-pin , 5-pin modes

For detailed information regarding the use of the SPI on the DM6467, see the *TMS320DM646x DMSoC Serial Peripheral Interface (SPI) User's Guide* (SPRUER4).

4.7 Phased-Locked Loop (PLL)/Clock Generators

The DM642 and DM6467 feature clock generators with PLLs that are used to generate clocks for these devices.

The DM642 clock generator has one PLL that can be used to generate a variety of different clocks from the device input clock. The PLL can multiply the input clock by 1, 6, or 12, based on the state of two input pins, and the resultant clock is divided by 1, 2, 4, and 8. These clocks are then used to satisfy the clocking requirements for the different parts of the DM642 device. Additionally, on the DM642 there is the option to use a separate external input signal to provide clock for the EMIF.

The DM6467 clock generator has two PLL controllers that provide clocks to different parts of the system. PLL1 provides clocks to most of the components of the DMSoC, while PLL2 is dedicated to the DDR2 memory controller. Each of these PLLs support a number of multiply and divide configurations, allowing the device to generate a number of different clock frequencies to satisfy a wide variety of system requirements.

Software controls the PLL1 operation through the system PLL Controller 1 Register (PLLC1) . The SYSCLK dividers are programmable and the AUXCLK is the clock provided to the fixed clock domains. The PLL1 multiplier is controlled by the PLLM bit in the PLL Multiplier Control Register (PLLM) and may be modified by software.

PLL2 provides the clock from which the DDR2 memory controller clock is derived. This is a separate clock system from the PLL1 clocks provided to other components of the system. This clock allows the reduction of the core clock rates to save power while maintaining the required minimum clock rate for DDR2. PLL2 must be configured to output a 2x clock to the DDR2 PHY interface. The SYSCLK divider is programmable and the auxiliary clock (AUXCLK) and SYSCLKBP are not used. The PLL2 multiplier may be modified by software.

For additional information regarding use of the PLL/clock generator on the DM6467, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

4.8 Universal Asynchronous Receiver/Transmitter (UART)

While the DM642 does not feature the UART peripheral, the DM6467 has three; therefore, this added capability can be utilized on the DM6467 systems.

The DM6467 UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. This module is capable of performing standard infrared communication in slow infrared (SIR) mode and medium infrared (MIR) mode defined by the Infrared Data Association (IrDA). The module supports a consumer infrared (CIR) communications mode that uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote control applications.

UART1 and UART2 feature flow control capability using the UART_RTS and UART_CTS signals. UART0, on the DM6467, additionally supports the following modem control signals: DCD, DSR, DTR, and RI. Table 11 describes the UART signals available on the DM6467.

Table 11. DM6467 UART Signal Descriptions

Signal	Pin	Type (1)	Description	Default
RX	URXD	I	Serial data input for all modes	Unknown
TX	UTXD	O	Serial data output in UART modes. In other modes, UTXD is set to the reset value (inactive state)	1
IRTX	$\overline{\text{URTS}}$	O	Serial data output in IrDA modes. In other modes, $\overline{\text{URTS}}$ is set to the reset value (inactive state) Pin multiplexed with RTS at the pin-out	0
RCTX	UTXD	O	Serial data output in CIR mode. In other modes, UTXD is set to the reset value (inactive state). Pin multiplexed with TX at the pin-out	0
$\overline{\text{CTS}}$	$\overline{\text{UCTS}}$	I	Clear to send. Active low modern status signal. Reading MSR[4] checks the condition of $\overline{\text{CTS}}$. Reading MSR[0] checks a change of state of $\overline{\text{CTS}}$ since the last read of MSR. $\overline{\text{CTS}}$ is used in autp-$\overline{\text{CTS}}$ mode to control the transmitter.	Unknown

(1) I = Input, O = Output

Table 11. DM6467 UART Signal Descriptions (continued)

Signal	Pin	Type [1]	Description	Default
$\overline{RTS}$	$\overline{URTS}$	O	Request to send. When active (low), $\overline{URTS}$ is ready to receive data. Setting MCR[1] activates $\overline{RTS}$. $\overline{URTS}$ becomes inactive as a result of a module reset, loop back mode or by clearing MCR[1]. In auto-$\overline{RTS}$ mode, it become inactive as a result of the receiver threshold logic	1
SD	$\overline{UCTS}$	O	SD mode is used to configure the transceivers. The SD pin-out is an inverted value of ACREG[6]. Pin multiplexed with CTS and the pin-out.	1
DSR	$\overline{UDSR0}$ [2]	I	Data set ready. Active-low modem status signal. Reading MSR[5] checks the condition of DSR. Reading MSR[1] checks a change of state of DSR since the last read of MSR.	Unknown
$\overline{DTR}$	$\overline{UDTR0}$ [2]	O	Data terminal ready. When active (low), $\overline{UDTR0}$ informs the modem that the module is ready to communicate. It's activated by setting MCR[0].	1
$\overline{DCD}$	$\overline{UDCD0}$ [2]	I	Data carrier detect. Active-low modem status signal. The condition of $\overline{DCD}$ can be checked by reading MSR[7] and any change in its state can be detected by reading MSR[3].	Unknown
$\overline{RI}$	$\overline{URIN0}$ [2]	I	Ring indicator. Active-low modem status signal. The condition of RI can be checked by reading MSR[6] and any change in its state can be detected by reading MSR[2].	Unknown

(2) Only supported on UART0

In UART mode, the module uses a wired interface for serial communication with a remote device. The module can be placed in an alternate mode (first-in-first-out (FIFO) mode) relieving the processor of excessive software overhead by buffering the received/transmitted characters. Both receiver and transmitter FIFOs can store up to 64 bytes of data (plus three additional bits of error status per byte for the receiver FIFO) and have selectable trigger levels.

The UART module is also capable of performing standard infrared communication in slow infrared mode and medium infrared mode defined by the IrDA. The module also supports consumer infrared communications, which uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote control applications.

The UARTs have dedicated interrupt signals to the ARM CPU and the interrupts are not multiplexed with any other interrupt source.

Table 12 lists the UART EDMA events available on the DM6467.

Table 12. DM6467 UART EDMA Events

Event	Acronym	Source
18	URXEVT0	UART0 Receive Event
19	UTXEVT0	UART0 Transmit Event
20	URXEVT1	UART1 Receive Event
21	UTXEVT1	UART1 Transmit Event
22	URXEVT2	UART2 Receive Event
23	UTXEVT2	UART2 Transmit Event

Pin multiplexing is utilized to accommodate the largest number of peripheral functions in the smallest possible package.

For detailed information regarding use of the UART peripherals on the DM6467, see the *TMS320DM646x DMSoC Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRUER6).

4.9 Timers

The DM642 and DM6467 feature several timers. The DM642 includes three 32-bit general purpose timers. The DM6467 includes two 64-bit general purpose timers, each configurable as two 32-bit timers and one 64-bit watchdog timer.

4.9.1 General-Purpose Timers

Since capability of the general-purpose (GP) timers on the DM642 and DM6467 is somewhat different, migrating an application to the DM6467 requires some modifications; however, because the DM6467 timers can be operated as four 32-bit timers, timer requirements of a DM642 application can easily be supported by the DM6467.

The DM6467 general-purpose timers actually support three modes of operation: a 64-bit general purpose timer, dual unchained 32-bit GP timers, and dual chained 32-bit timers. The GP timer modes can be used to generate periodic interrupts or EDMA synchronization events.

Configuring the DM6467 timers in 32-bit unchained mode allows straightforward migration of DM642 timer requirements to this device. Although configuration and pinouts differ, the timer capabilities of the DM6467 map well to support the timer requirements of a DM642 application.

Table 13 presents a comparison between the timers on the DM642 and the DM6467, when the DM6467 timers are partitioned in 32-bit mode.

Table 13. General-Purpose Timer Comparison

Timer Features	DM642	DM6467
Number of 32-bit timers	3	4
Number of possible timer events	3	2
Number of separate clock inputs	2	
Number of separate timer outputs	2	

For detailed information regarding use of the DM6467 general purpose timers, see the *TMS320DM646x DMSoC 64-Bit Timer User's Guide* (SPRUER5).

4.9.2 Watchdog Timer

The DM6467 features a watchdog timer, while the DM642 does not, therefore, the DM6467 systems may benefit from this added functionality. The watchdog timer can be extremely useful, especially in real-time systems, to allow the capability to recover in case of unexpected events that might otherwise cause the system to stop functioning properly.

Timer2 on the DM6467 can be configured only as a 64-bit watchdog timer. As a watchdog timer, it can be used to prevent system lockup when the software becomes trapped in loops with no controlled exit. In other words, the watchdog timer allows the capability to interrupt or reset the device if the watchdog timer is not serviced at a programmable interval.

For detailed information regarding the use of the DM6467 watchdog timer, see the *TMS320DM646x DMSoC 64-bit Timer User's Guide* (SPRUER5).

4.10 Ethernet Media Access Controller (EMAC)

The DM642 and DM6467 feature an IEEE 802.3 compliant, Ethernet media access controller (EMAC) peripheral that provides Ethernet interface capability. The Ethernet interface is comprised of the EMAC and the physical layer (PHY) device management data input/output (MDIO) module. The EMAC controls the flow of packet data from the DSP to the PHY while the MDIO module controls the PHY configuration and status monitoring.

The DM642 device provides support for the 10/100/ Mbps Ethernet interface. The DM6467 EMAC module features a synchronous 10/100 Mbps operation in either half-duplex or full-duplex mode with a standard media independent interface (MII) to the PHY and a synchronous 1000 Mbps operation in full-duplex mode with a Gigabit media independent interface (GMII) to the PHY.

The frequencies for transmit and receive clocks are fixed by the IEEE 802.3 specifications. These clocks are inputs to the EMAC module that operate at 2.5 MHz in 10-Mbps mode, 25 MHz in 100-Mbps mode, and 125 MHz in 1000-Mbps mode (DM6467 only).

The EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to control device reset, interrupts, and system priority.

The DM642 and DM6467 EMAC control modules include 8K bytes of internal memory, which is essential for allowing the EMAC to operate more independently of the CPU. The bus arbiter is used to arbitrate between the CPU and EMAC buses for access to internal descriptor memory and internal EMAC buses for access to system memory.

The DM6467 control module has four separate interrupt signals. The four separate sources of interrupt on the DM6467 can be individually enabled for each channel by the Receive Threshold Interrupt Enable Register (CMRXTHRESHINTEN), Receive Interrupt Enable Register (CMRXINTEM), Transmit Interrupt Enable Register (CMTXINTEN), and Miscellaneous Interrupt Enable Register (CMMISCINTEN). Table 14 shows the DM6467 control module interrupts.

Table 14. DM6467 EMAC Control Module Interrupts

Event	Acronym	Source
24	MAC_RXTH	EMAC Receive Threshold
25	MAC_RX	EMAC Receive
26	MAC_TX	EMAC Transmit
27	MAC_MISC	EMAC Miscellaneous

The DM6467 control module features interrupt pacing for receive and transmit pulse interrupts. The receive threshold and miscellaneous interrupts cannot be paced. The interrupt pacing feature limits the number of interrupts to the CPU during a given period of time. For heavily loaded systems in which interrupts can occur at a very high rate, the performance benefit is significant due to minimizing the overhead associated with servicing each interrupt.

The DM6467 module uses the same pins for the MII and GMII modes of operation, however, only one mode can be used at a time. The EMAC on the DM6446 and the DM6467 can only be controlled by the ARM CPU.

For more detailed information regarding the use of the EMAC on the DM6467, see the *TMS320646x DMSoC Ethernet Media Access Controller (EMAC)/ Management Data Input/Output (MDIO) Module User's Guide* (SPRUEQ6).

4.11 Inter-Integrated Circuit (I2C) Interface

The DM642 and DM6467 feature interface to I2C compatible external devices. The basic I2C functionality provided by the DM642 and the DM6467 is the same, however, the actual I2C peripheral module and register set are different between these two devices.

The I2C module on the DM642 and DM6467 feature:

- Compliance with Philips Semiconductors I2C-bus specification (version 2.1)
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- Free data format mode
- One read DMA event and one write DMA event that the DMA can use
- Peripheral enable/disable capability

In addition, the I2C peripheral modules are capable of generating interrupts. Table 15 describes the interrupts generated by the DM6467.

Table 15. DM6467 I2C Interrupt Events

I2C Interrupt	Initiating Event
Arbitration-lost interrupt (AL)	Generated when the I2C arbitration procedure is lost or illegal START/STOP conditions
No-acknowledge interrupt (NACK)	Generated when the master I2C does not receive any acknowledge from receiver
Registers-ready-for-access interrupt (ARDY)	Generated by the I2C when the previously programmed address, data, and command have been performed and the status bits have been updated. This interrupt is used to let the controlling processor know that the I2C registers are ready to be accessed.
Receive interrupt/status (ICRINTP)	Generated when the receives data in the receive-shift register (ICRSR) has been copied into the ICDRR. The ICRRDY bit can also be polled by the CPU to read the received data in the ICDRR.
Transmit interrupt/status (ICXINT and ICXRDY)	Generated when the transmitted data has been copied from ICDXR to the transmit-shift register (ICXSR) and shifted out on the SDA pin. This bit can also be polled by the CPU to write the next transmitted data into the ICDXR.
Stop-condition-detection interrupt (SCD)	Generated when a STOP condition has been detected
Address-as-slave interrupt (AAS)	Generated when the I2C has recognized its own slave address or an address of all (8) zeros.

The DM6467 I2C peripheral is also capable of interrupting the ARM CPU. The CPU can determine which I2C events caused the interrupt by reading the I2C Interrupt Vector Register (ICIVR).

Table 16. DM6467 I2C ARM Interrupt

ARM Event	Acronym	Source
39	I2CINT	I2C

The I2C interrupt to the ARM CPU is not multiplexed with any other interrupt source. For detailed information regarding the use of the I2C module on the DM6467, see the *TMS320DM646x DMSoC Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUER0).

4.12 VLYNQ

The DM6467 features a VLYNQ™ communications interface product, while the DM642 does not, therefore, DM6467 systems may benefit from this added functionality. VLYNQ is a serial interface with a low pin count, high-speed point-to-point serial interface used for connecting-to-host processors and other VLYNQ compatible devices. This interface can be implemented in either a host-to-peripheral or peer-to-peer fashion.

The VLYNQ port is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference. VLYNQ enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped to local physical address space and appear as if they are on the internal bus of the DM6467. The external devices must also have a VLYNQ interface.

VLYNQ uses a simple block code (8b/10b) packet format and supports in-band flow control so that no extra terminals are needed to indicate that overflow conditions might occur. The external device can also initiate read and write transactions.

For detailed information regarding the use of the DM6467 VLYNQ port, see the *TMS320DM646x DMSoC VLYNQ Port User's Guide* (SPRUER8).

4.13 Host Port Interface (HPI)

The DM642 and DM647 feature an HPI that enables an external host processor to directly access program/data memory using a parallel interface. The primary purpose is to provide a mechanism to move data to and from the processor. The HPI interfaces used on these devices are similar in function and pinout; however, the DM642 and DM6467 contain different versions of the HPI module. To migrate an application from a DM642 to a DM6467, some software and hardware interconnection changes are required.

The external HPI interface signals implement a flexible interface to a variety of host devices. Through the DM642 HPI, an external host is capable of accessing the entire DSP memory map except for interrupt selector registers and emulation logic. The DM6467 HPI can be used by the host to access HPI configuration registers, DDR2 memory controller configuration register file and memory address ranges, Power and Sleep Controller Registers (PSC), PLL0 and PLL1 registers, ARM internal memory, CPU internal memory, and VLYNQ remote memory. Table 17 describes the signals available of the DM642 and DM6467.

Table 17. DM642 and DM6467 UART Signal Descriptions

DM642 Signal	DM6467 Signal	Signal Type (1)	Host Connection	Function
HCNTL[1-0]	HCNTL[1:0]	I	Address or control lines	HPI access control input
$\overline{\text{HCS}}$	$\overline{\text{HCS}}$	I	Chip select Pin	HPI chip select
HR/$\overline{\text{W}}$	HR/$\overline{\text{W}}$	I	R/W strobe pin	HPI read/write
HHWIL	HHWIL	I	Address or control pins	Halfword identification line (only in dual-halfword mode)
$\overline{\text{HAS}}$	$\overline{\text{HAS}}$	I	None	Address strobe
$\overline{\text{HINT}}$	$\overline{\text{HINT}}$	O/Z	Interrupt pin	Host interrupt
$\overline{\text{HDS[1-2]}}$	$\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$	I	Read strobe and write strobe pins or any data strobe pin	HPI data strobe pins
HD[15-0] or HD[31-0]	HD[x:0]	I/O/Z	Data bus	HPI data bus
$\overline{\text{HRDY}}$	$\overline{\text{HRDY}}$	O/Z	Asynchronous ready pin	HPI-ready signal

(1) I = Input, O = Output, Z = Hi-Impedance

The DM642 and DM6467 feature dual 16-bit half-word cycle access (internal data word is 32-bits wide) and 32-bit word cycle access (internal data word is 32-bits wide). The DM6467 also features internal data bursting using 8-word read and write FIFO buffers.

The DM6467 has a single interrupt source to both the ARM and DSP CPUs that is not multiplexed with any other interrupt sources on either CPU.

Table 18. DM6467 I2C ARM Interrupt

ARM Event	Acronym	Source
23	HPIINT	HPI

For detailed information regarding the use of the HPI interface on the DM6467, see the *TMS320DM646x DMSoC Host Port Interface (HPI) User's Guide* (SPRUES1).

4.14 General-Purpose Input/Output (GPIO)

The DM642 and DM6467 feature a selection of pins that can be configured to provide independent single-bit general-purpose digital input/output (GPIO). Since the GPIO configuration differs between these two devices, software modifications are necessary to migrate from the DM642 to the DM6467.

Specifically, the DM642 features up to 16 GPIO pins and the DM6467 features up to 33 GPIO pins. These GPIO pins can be used to interface to external signals, and to generate interrupts.

On the DM642 all GPINTn are synchronization events to the EDMA, however, only GPINT0 and GPINT [4-7] are available as interrupts to the CPU. All DM6467 GPIO signals can be used as interrupt sources and generate events to the EDMA. The DM6467 GPIO peripheral can send interrupt events to the ARM and/or the DSP. Interrupts from DM6467 GPIO signals at both independent and group level is supported.

Additionally, on both devices, many GPIO pins are multiplexed with other pin functions; therefore, GPIO pin availability depends on what other functions are used on the device.

For detailed information regarding the use of the GPIO interface on the DM6467, see the *TMS320DM646x DMSoC General-Purpose Input/Output (GPIO) User's Guide* (SPRUEQ8).

4.15 Pulse-Width Modulation (PWM)

The DM6467 features the pulse width modulator (PWM) peripheral, while the DM642 does not. This added capability can be utilized in DM6467 systems. There are two identical instances of the PWM on the DM6467 device: PWM0 and PWM1.

The DM6467 PWM provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter (DAC) with some external components. Each PWM output is implemented as a timer with a period counter and a first-phase duration comparator, where the bit widths of the period and first-phase duration are both programmable. The period and the first-phase duration are controlled with 32-bit counters, and each PWM output can also be used to generate and interrupt and/or EDMA sync event.

For detailed information regarding the use of the PWM on the DM6467, see the *TMS320DM646x DMSoC Pulse-Width Modulator (PWM) User's Guide* (SPRUER3).

4.16 Universal Serial Bus (USB) Interface

The DM6467 features a USB controller that can be used as either a host or a peripheral. As a host, it supports all three speeds: low (1.5 Mbps), full (12 Mbps), and high (480 Mbps) in point-to-point data transfers with another peripheral or device or multiple peripherals/devices via a HUB in a multipoint set-up. As a peripheral, it supports high-speed (480 Mbps) and full-speed (12 Mbps) operations.

Table 19 presents the USB pins available on the DM6467.

Table 19. DM6467 USB Pins

Pin	Type (1)	Function
AUX_MXI/AUX_CLKIN	I	Crystal input for AUX oscillator
AUX_MXO	O	Crystal output for AUX oscillator
AUX_DV_{DD18}	S	1.8 V power supply for AUX oscillator I/O
AUX_CV_{DD}	S	1.2 V power supply for AUX oscillator
AUX_DV_{SS}	GND	Ground for AUX oscillator I/O
AUX_V_{SS}	GND	Ground for AUX oscillator. Connect to crystal load capacitors. Do not connect to board ground (V_{SS}).
USB_DP	A I/O	USB data differential signal pair (positive/negative)
USB_DN	A I/O	USB data differential signal pair (positive/negative)
USB_R1	A I/O	USB current reference. This must be connected via a 10kΩ ± 1% resistor to USB_VSSREF
USB_DRVVBUS/GPIO22	I/O	When used for USB and the USB controller is operating as a host, this signal is driven by the USB controller to enable the external VBUS charge pump.
USB_V_{SSREF}	GND	Ground for current reference
USB_V_{DDA3P3}	S	Analog 3.3 V power supply for USB
USB_V_{DD1P8}	S	1.8 V I/O power supply for USB
USB_$V_{DD1P2LDO}$	S	USB core power supply LDO regulator output. This must be connected via 1 µF capacitor to ground. Do not connect this to other supply pins.

(1) A = Analog Signal, GND = Ground, I = Input, O = Output, R = Reference Voltage, S = Supply Voltage

When the USB controller assumes the role of a host, it is required to supply a 5 V power to an attached device through its VBUS line. To achieve this task, the USB controller requires the use of an external logic (or charge pump) capable of sourcing a 5 V power. The USB_DRVVBUS is used as a control signal to enable/disable the external logic to either source or disable power on the VBUS line.

On the DM6467 DMSoC, there is no connection to PHY VBUS input since On-The-Go (OTG) is not supported. Since the OTG feature is not supported, controller behavior as a host or peripheral is not evaluated by hardware automatically via cabling. Instead, you need to program the USBID bit of the USBTCL register in the system module to select the USB as a host or a peripheral. The USB controller is operated by ARM through the memory mapped registers.

For more detailed information on the USB interface, see the *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller User's Guide* (SPRUER7).

4.17 ATA/ATAPI Interface

The DM6467 features an AT attachment/ATA packet interface (ATA/ATAPI), also known as IDE controller, while the DM642 does not. This added capability can be utilized on DM6467 systems.

The DM6467 supports an onboard ATA host controller module allowing it to exploit access to a vast majority of available data storage and audio devices. The onboard IDE host controller performs PIO, multiword, and ultra-DMA transactions with ATA and ATAPI compliant devices. Hard-disk drive, compact disk, compact flash, and DVD are members of ATA/ATAPI compliant devices that the IDE host controller is destined to interface with.

The DM6467 ATA controller has the following features:

- Single channel capable for connecting up to two ATA/ATAPI devices
- Supports interface to compact Flask configured in true-IDE mode
- Supports PIO modes 0,1,2,3, and 4
- Supports multiword DMA modes 0,1, and 2
- Supports ultra-DMA modes 0,1,2,3,4, and 5
- Full scatter gather DMA capability
- Programmable timing parameters provide support of any multiple ATA timing options mode at any processor clock frequency

For detailed information regarding the use of ATA controller on the DM6467, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (SPRUEQ3).

5 Interrupt Considerations

The DM642 and DM6467 both support servicing of a wide range of interrupts from a variety of sources, both on- and off-chip. Each device uses its own multiplexing scheme to select the specific sources that will actually be allowed to interrupt the CPU.

The DM642 accepts a total of 16 independent interrupt inputs to the CPU, but allows these interrupts to be chosen from a possible selection of 32 sources in addition to four interrupts which are always selected, allocated to reset, NMI, and two reserved interrupts. The 32 possible interrupt sources are mapped to 12 independent interrupts using the MUXH and MUXL registers. The resultant 16 interrupt signals are sent to the CPU. The polarities of the selected input signals which will actually generate interrupts are programmable through the EXTPOL register.

On the DM6467 both the ARM and the C64x+ are capable of servicing interrupts; however, all of the device interrupts are routed to the ARM interrupt controller with only a limited set routed to the C64x+ interrupt controller. The interrupts can be selectively enabled or disabled in either of the controllers. In typical applications, the ARM handles most of the peripheral interrupts and grants control to the C64x+, of interrupts that are relevant to DSP algorithms. Also, the ARM and DSP can communicate with each other through interrupts.

The DM6467 ARM CPU core accepts two basic interrupts, a normal interrupt request (IRQ) and a fast interrupt request (FIQ). There are up to 64 possible total interrupt sources supported by the ARM interrupt architecture. There are 60 interrupt sources used on the DM6467 device. These interrupt sources are multiplexed to either the IRQ and or FIQ interrupt, at eight different priority levels. This multiplexing and the interrupt priority level assignments are controlled by bits in the various interrupt controller registers.

When one of these interrupts occurs, it is prioritized against any other pending and enabled interrupts, and sent to the ARM as either an IRQ or an FIQ. The ARM CPU then reads the address of the appropriate interrupt service routine to branch to from the interrupt entry table, loaded by the processor initialization routine. In this way, any of the possible interrupts may be serviced.

On the DM6467 DSP CPU core, sources that are allowed to interrupt the CPU may be chosen from a possible selection of 128 system events, in addition to three interrupts which are always selected, allocated to reset, NMI, and a hardware exception interrupt. The 128 possible system events are mapped to 12 independent interrupts using the interrupt selector, interrupt combiner, and exception combiner modules. The resultant 15 interrupt signals are sent to the CPU. Some of the possible interrupts on the DSP CPU can be generated from GPIO signals, and the polarities of these signals used to generate the interrupts are programmable through the GPIO control registers.

The 128 system event sources from which the 12 interrupts routed to the CPU are chosen or hard-wired on the DM6467. The interrupts that are actually routed to the CPU in the device is chosen from this selection as described above. This interrupt selection structure allows for maximum flexibility within the system for allocation of necessary interrupt servicing.

For detailed information regarding the handling of interrupts on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403), the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8), and the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

6 Bootloading Capabilities

The DM642 and the DM6467 provide the capability to transfer code from an external location into RAM to be executed following reset. On both devices, the states of various input pins are sampled following reset, and the selected boot modes are determined based on these states.

The DM642 provides three boot modes: host boot through PCI or HPI, EMIF boot, and no boot. These boot modes are selected by the state of the AEA[22:21] and PCI_EN pins following reset. In the host-boot mode, the host device serves as the master for the bootload operation. In the EMIF-boot mode, the DMA controller automatically copies 1K of data from the CE1 space to internal memory starting at location zero. The DM642 does not contain the bootloader program.

The DM6467 ARM CPU provides seven bootload modes: host boot loading through the HPI, EMIF bootloading from NAND flash, serial bootloading through UART0, PCI-boot mode (with auto-initialization/ without auto-initialization), master I2C-boot mode using Application Image Script (AIS) format, SPI-boot mode using AIS, and EMIFA-boot mode. The EMIFA-boot mode does not transfer any code, but instead, branches directly to an external location (0x42000000) in NOR flash memory where it expects code.

For host bootloading through the HPI, the ARM bootloader expects that the code to be executed is loaded through the HPI by an external host and branches to this code once loading is completed. If EMIFA or serial bootloading is selected, the bootloader loads the code provided through either interface by an external device and then transfers control to this code.

The ARM-boot modes are selected by the BTMODE[3:0] pins, and when EMIF booting is used the address bus width of the EMIF are selected by the CS2BW pins.

For detailed information regarding use of the ARM bootloader, see *Using the TMS320DM6467 DMSoC Bootloader* (SPRAAS0).

There is one boot mode on the DM6467 DSP CPU core. The DSPBOOT input determines DSP operation at reset. When DSPBOOT = 1, the DSP will boot itself. Under this scenario, DSP is released from reset without ARM intervention. The DSP boot address is set to an EMIFA address 0x4220 000h. DSP begins execution with instruction (L1P) cache enabled.

The DSPBOOT operation is overridden when ARM HPI or PCI boot is selected (BTMODE [3:0] = 001x). This is because ARM HPI/PCI boot selection forces the HPIEN or PCIEN bit in PINMUX0 to '1'. This enables UHPI/PCI functions of the EMIFA control and data pins and prevents the DSP from using EMIFA. DSPBOOT is treated as '0' internally when BTMODE [3:0] = 001x, regardless of the value at the configuration pin (The actual pin value should still be latched in the BOOTCFG register of the system module).

For more information on the DSP boot mode, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

7 Power Management

In most DSP systems, power management is an important concern to allow DSP functions to perform with the lowest power cost and minimal battery drain possible. The DM642 and DM6467 offer numerous options for power management. The devices provide several basic categories of power management options with variations.

On the DM642, there are three basic options for power management. The first involves peripherals that are enabled and disabled depending on the state of external input pins. These peripherals are the PCI, HPI, and the EMAC. The state of the PCI_EN, MAC_EN, and HD5 pins determines which of these peripherals is enabled.

The second power management option is controlled by the bits in the Peripheral Configuration Regsiter (PERCFG). This register contains bits that can be used to enable or disable the McASP, McBSP, video port, and I2C peripherals. The third power management option on the DM642 is controlled by bits in the Control Status Register (CSR). These bits can be used to selectively enable or disable the CPU, peripherals, or PLL.

The DM6467 DMSoC has a single power domain, the *Always On* power domain. Within this domain, the PSC controls device power by gating off clocks to individual peripherals/modules. The PSC is composed of the global PSC (GPSC) module which contains memory-mapped registers, PSC interrupt control, and a state machine for each peripheral/module. A local PSC (LPSC) is associated with each peripheral/module and provides clock and reset control. The GPSC controls all of the LPSCs.

The DM6467 ARM subsystem does not have an LPSC module. ARM sleep mode is accomplished through the wait for interrupt instruction. Table 20 presents a comparison of the possible LPSC peripheral/module allocation assignments on the DM6467.

Table 20. LPSC Peripheral/Module Allocation Assignment Comparison

LPSC Number	DM6467
0	Reserved
1	C64x+ CPU
2	HDVICP0
3	HDVICP1
4	EDMACC
5	EDMATC0
6	EDMATC1
7	EDMATC2
8	EDMATC3
9	USB
10	ATA
11	VLYNQ
12	HPI
13	PCI
14	EMAC/MDIO
15	VDCE
16	Video Port

Table 20. LPSC Peripheral/Module Allocation Assignment Comparison (continued)

LPSC Number	DM6467
17	Video Port
18	TSIF0
19	TSIF1
20	DDR2 Memory Controller
21	EMIFA
22	McASP0
23	McASP1
24	CRGEN0
25	CRGEN1
26	UART0
27	UART1
28	UART2
29	PWM0
30	PWM1
31	I2C
32	SPI
33	SPI
34	GPIO
35	TIMER0
36	TIMER1
37	Reserved
38	Reserved
39	Reserved
40	Reserved
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Reserved

To manage power due to I/O buffers on the device, the DM6467 also has the capability to power up or down groups of I/O pin buffers. This feature is controlled by writing to bits in the VDD3PDV_PWDN register. Note that this register controls only the power supply to the 3.3 V I/O buffers for each designated group of pins. The PSC determines the clock/power state of the peripheral.

The USB PHY can be powered down when not in use. The USB PHY is powered down via the DM6467 PHYDWN bit in the USB Control Register (USBCTL) of the control module. USBCTL is described in the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403). Table 21 summarizes the power management features on the DM6467.

Table 21. DM6467 Power Management Features

Power Management Features	Description
Clock Management	
PLL power-down	The PLLs can be powered down when not in use to reduce switching power
Module clock ON/OFF	Module clocks can be turned on/off to reduce switching power
Module clock frequency scaling	Module clock frequency can be selected to reduce switching power
ARM and DSP Sleep Management	
ARM Wait-for-Interrupt Sleep Mode	Disable ARM clock to reduce active power

Table 21. DM6467 Power Management Features (continued)

Power Management Features	Description
	Clock Management
DSP sleep modes	The DSP can be put into sleep mode to reduce switching power
3.3 V I/O powerdown	The 3.3 V I/Os can be powered down to reduce I/O cell power
	I/O Management
USB Phy powerdown	The USB Phy can be powered down to reduce USM I/O power

For more details on the DM6467 power management, see the *TMS320646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

8 PLL/Clock Modes at Reset

The DM642 and DM6467 feature flexible clock generators that provide clocking to satisfy a wide variety of system requirements. To properly start up and initialize a DSP system, the clock generator must be able to provide appropriate clock signals to the device even before the device is released from reset. The DM642 and DM6467 clock generators are designed to provide this capability.

The DM642 has two clock mode pins (CLKMODE[1:0]) that are used to select the clock mode at reset. These two pins select between a multiply by 1, 6, or 12 of the device input clock, the result of which is then used to provide clocks to the device until this selection is changed and the device is reset again. On the DM642, the input clock frequency range is 30 MHz - 75 MHz.

The DM6467 can be clocked either by an external oscillator, or by using a crystal with the internal oscillator. The internal oscillator is enabled by default when reset is asserted, but can be disabled through software by writing to the PLL Controller 1 PLL Control Register (PLLCTL), if desired. The default clock mode for the DM6467 at reset is a multiply by 1 of the input clock. Once the device is released from reset, the clock frequency can be changed through software by writing to registers in the PLL module. The input clock frequency range on the DM6467 is 20 MHz - 30 MHz.

Table 22 presents a comparison of the DM642 and DM6467 PLL and clock mode initialization.

Table 22. DM642 and DM6467 PLL/Clock Modes at Reset

Features	DM642	DM6467
Input clock frequency range	30 MHz - 75 MHz	20 MHz - 30 MHz
On-chip oscillator	No	Yes (1)
Clock mode at reset	x1, x6 or x12	x1, oscillator enabled
Clock mode at reset determined by	CLKMODE[1:0] pins	Not Variable (2)
Software can change clock rate after reset	No	Yes

(1) (1) Oscillator is on by default. Turn it off in software after reset, if desired.
(2) (2) Bootloader may change clock frequency after resets, see Section 6.

For detailed information regarding PLL and clock mode initialization, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403) and the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8).

9 Pin Multiplexing

The DM642 and the DM6467 use multiplexing of functions on various pins to maximize device features and flexibility, while minimizing pin count, and, therefore, package size and cost. Pin multiplexing is accomplished in a similar fashion on both devices; however, the actual implementation on each device is different, therefore, software changes may be necessary. Consult the DM6467 documentation for operational details.

Functionally, on both devices, the default pin multiplexing configuration is determined by the state of various input pins at reset, and the reset state of various register bits. Following reset, the pin multiplexing configuration can be modified through software by writing to various registers.

On the DM6467, the pin multiplexing configuration following reset is controlled through software using two dedicated registers: Pin Multiplexing Control 0 (PINMUX0) and Pin Multiplexing Control 1 (PINMUX1). Writing to these two registers can be used to modify the pin multiplexing configuration to suit a wide variety of system applications.

The following peripherals have multiplexed pins on the DM6467: VPIF, transport stream interface (TSIF0), TSIF1, clock reference generator (CRGEN0), CRGEN1, EMIFA, PCI, HPI, ATA, PWM0, PWM1, UART0, UART1, UART2, Audio Clock Selector, the USB USB_DRVVBUS pin, and GPIO.

For detailed information regarding pin multiplexing and its control on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403) and the device-specific user's guides for the specific peripherals being used.

10 Power Supplies

The DM642 and DM6467 utilize multiple power supplies to maximize flexibility, performance, and minimize power dissipation, as well as to adhere to industry standards for various external interfaces.

The DM642 utilizes an industry standard 3.3 V power supply for its I/O pins, and either a 1.2 V supply for the 500 MHz operation, or a 1.4 V supply for the DM642A and 600MHz/700 MHz versions of the DM642.

The DM6467 utilizes a 3.3 V supply for its I/O pins, and either a 1.2 V core supply for 594 MHz or 729 MHz operation, or a 1.05 V core supply for 594 MHz operation only. Additionally, the DM6467 also requires a 1.8 V supply for the DDR2 interface, and for the device PLLs. Table 23 summarizes the power supply requirements for the DM642 and the DM6467.

Table 23. Power Supply Requirements at Reset

Supply		DM642	DM6467
Core	Voltage	1.2 V (500 MHz) 1.4 V (A500/A600/600/720 MHz)	1.2 V (594/729 MHz), 1.05 (594 MHz)
I/O 1	Voltage	3.3 V	3.3 V
I/O 2	Voltage	NA	1.8 V

For detailed information regarding power supply requirements on the DM6467, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

11 Package and Pin Count Comparisons

The DM642 and DM6467 are both provided in cost-efficient, high density BGA packages. Since the two devices have different pin-outs, the pin connections and locations are different between the two devices, therefore, PC board layout and signal connection modifications are necessary. Table 24 shows a comparison of the packages and pin counts for the DM642 and the DM6467.

Table 24. Package/Pin Count Comparison

Characteristic	DM642	DM6467
Designator	548 pin ZDK (Pb-free), GDK	529 pin ZUT (Pb-Free)
Ball Pitch	0.8 mm	0.8 mm
Dimensions	23 x 23 mm	19 x 19 mm
Maximum Case Temperature	90°C (default) 105°C (A version)	85°C -40°C - 105°C (A version)
Designator	548 pin ZNZ (Pb-free), GNZ	
Ball Pitch	1.0 mm	
Dimensions	27 x 27 mm	
Maximum Case Temperature	90°C (default) 105°C (A version)	

For detailed information regarding pin-out and mechanical dimensions of the DM6467 packages, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

12 References

- TMS320DM642 - http://focus.ti.com/docs/prod/folders/print/tms320dm642.html
- TMS320DM6467 - http://focus.ti.com/docs/prod/folders/print/tms320dm6467.html
- *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403)
- *TMS320C64x to TMS320C64x+ CPU Migration Guide* (SPRAA84)
- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732)
- *ARM926EJ-S Technical Reference Manual*, available at: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0198e/index.html
- *TMS320C64x+ DSP Cache User's Guide* (SPRU862)
- *TMS320646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9)
- *TMS320DM646x DMSoC DDR2 Memory Controller User's Guide* (SPRUEQ4)
- *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (SPRUEQ7)
- *EDMA v3.0 (EDMA3) Migration Guide for TMS320DM644x DMSoC* (SPRAAA6)
- *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUEQ5)
- *TMS320DM646x DMSoC Peripheral Component Interconnect (PCI) User's Guide* (SPRUER2)
- *TMS320DM646x DMSoC Multichannel Audio Serial Port (McASP) User's Guide* (SPRUER1)
- *TMS320DM646x DMSoC Serial Peripheral Interface (SPI) User's Guide* (SPRUER4)
- *TMS320DM646x DMSoC Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRUER6)
- *TMS320DM646x DMSoC 64-bit Timer User's Guide* (SPRUER5)
- *TMS320646x DMSoC Ethernet Media Access Controller (EMAC)/ Management Data Input/Output (MDIO) Module User's Guide* (SPRUEQ6)
- *TMS320DM646x DMSoC Inter-Integrated Circuit (I2C) Module User's Guide* (SPRUER0)
- *TMS320DM646x DMSoC VLYNQ Port User's Guide* (SPRUER8)
- *TMS320DM646x DMSoC Host Port Interface (HPI) User's Guide* (SPRUES1)
- *TMS320DM646x DMSoC General-Purpose Input/Output (GPIO) User's Guide* (SPRUEQ8)
- *TMS320DM646x DMSoC Pulse-Width Modulator (PWM) User's Guide* (SPRUER3)
- *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller User's Guide* (SPRUER7)
- *TMS320DM646x DMSoC ATA Controller User's Guide* (SPRUEQ3)
- *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8)
- *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871)
- *Using the TMS320DM6467 DMSoC Bootloader* (SPRAAS0)

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