Application Report
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Multi-Media Card (MMC) DLL Tuning

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ABSTRACT

This application report describes how to perform DLL tuning with Multi-Media Cards (MMCs) at 192 MHz (SDR104, HS200) on the OMAP5, DRA7xx, TDA2xx, and AM57xx family of devices. The document describes why the tuning algorithm is needed and how it works to achieve a functional system.

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1 DLL Tuning Algorithm Overview

The DLL read tuning algorithm is recommended by SD Group and JEDEC Solid State Technology Association to compensate for timing variations due to a collection of system factors at 192 MHz high speed of operation. These factors include changes in silicon processes, operating temperature and voltage, PCB loading, as well as eMMC memory device output timing.

During the 192 MHz (SDR104 for SD, HS200 for JEDEC) read tuning process, the CLK-DAT latching position is adjusted through the DLL in steps of 4, through a range of 125 ratio elements. At each tuning step, if the resultant delayed CLK, MMC_DLL_CLK, falls within the data valid window, then the result is a tuning pass at that tuning step. If not, then data is read incorrectly due to CLK-DAT setup/hold time violations, and the result is marked with tuning error. The 125 ratio elements constitute a delay duration of more than a full clock cycle, when running at 192 MHz. As a result, it is expected that two ranges of tuning ratio elements will be marked with tunning errors, on each side of a passing window, when tuning through the full range of ratio elements.

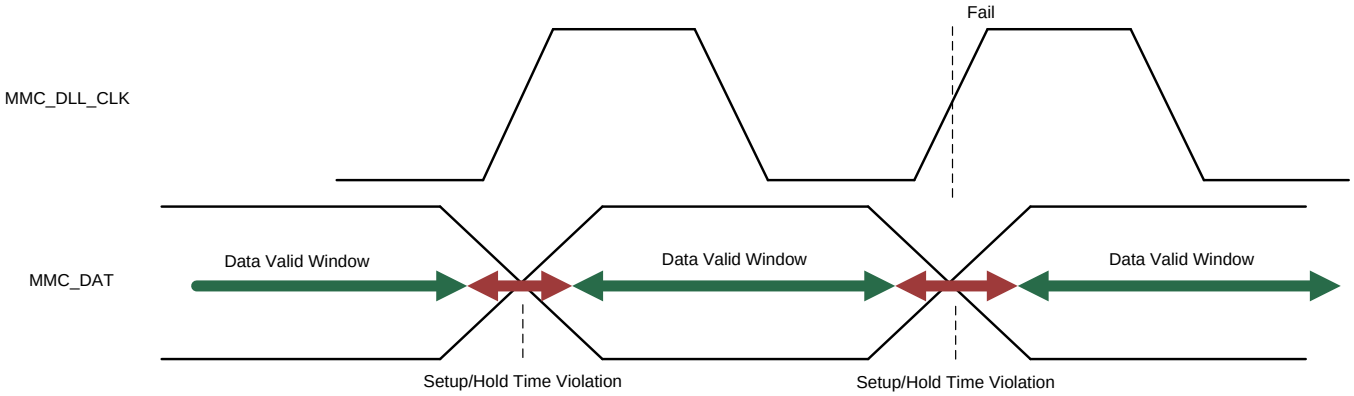

Figure 1. Setup and Hold Time Requirements

The requirement causes band errors 1 and 2 to occur as marked in the tuning results with 125 ratio elements. This is expected behavior.

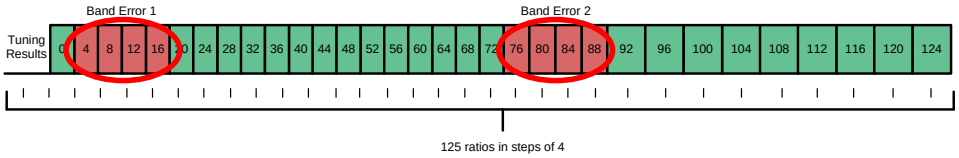

Figure 2. Tuning Band Error

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2 Tuning Re-Timing Error

On applicable devices, a second stage latch is used to re-capture data captured by MMC_DLL_CLK. The second stage latch captures with the original transmitting clock, MMC_CLK.

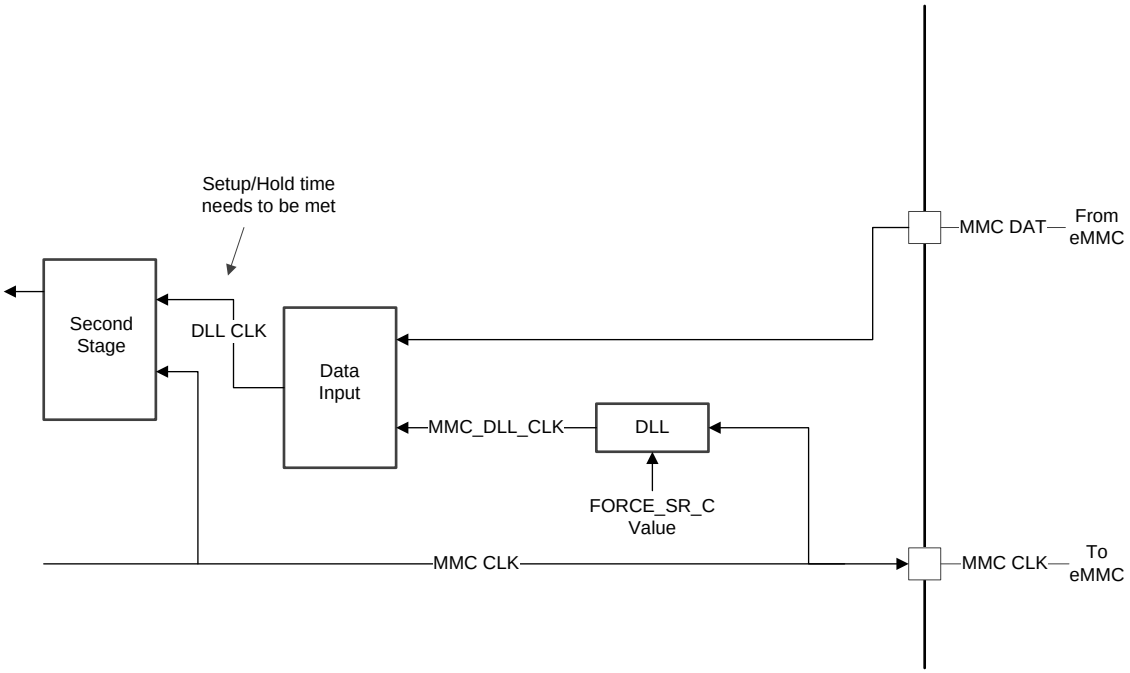

Figure 3. Simplified SoC 192 MHz Mode DLL Block Diagram

MMC_DLL_CLK and MMC_CLK both run at the same clock frequency; as a result, a narrow range of tuning delay elements may delay MMC_DLL_CLK to where it aligns in phase with MMC_CLK. Should the clocks come in phase, the data captured by the first clock will violate the setup and hold time requirements needed for the second stage latch; hence resulting in incorrectly read data. This is represented by re-timing error shown in Figure 4.

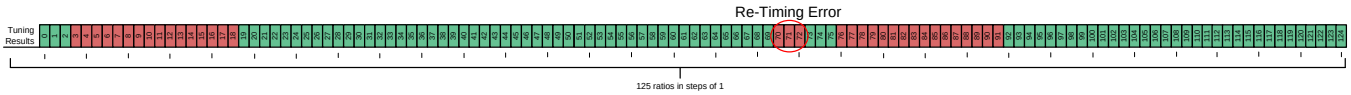

Figure 4. Tuning Re-Timing Error

By taking the entirety of 125 ratio elements into perspective, a tuning re-timing error can best be identified by a narrow range of DLL ratio elements that incorrectly read back tuning data.

Tuning *re-timing errors* are narrow in width. A DLL tuning algorithm that implements tuning with 4-step increments may miss a bad tuning delay value and predict an incorrectly large passing tuning window.

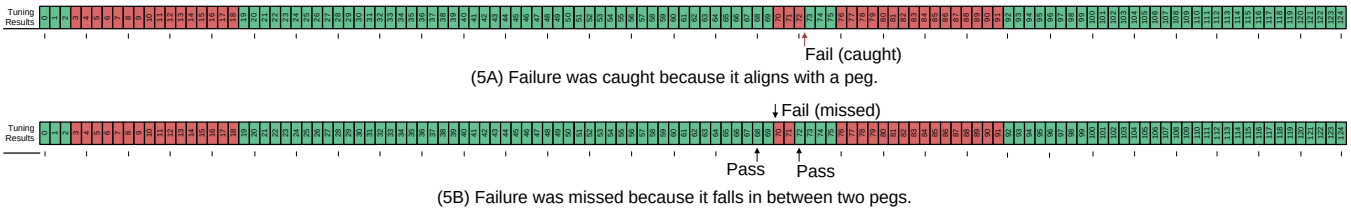

Figure 5. Re-Timing Error Caught vs Missed

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2.1 Tuning Re-Timing Error Voltage and Temperature Dependencies

Tuning *re-timing error* shifts to a smaller value when temperature increases, and a larger value with higher vdd (core) supply voltage. This behavior can be utilized in the workaround.

For systems in which legacy MMC DLL tuning algorithm [(1)] choses a ratio less than 40, which is sufficiently far from the lowest re-timing error ratio element, no workaround is necessary.

3 Software Tuning Algorithm

DLL tuning algorithm has been optimized to work around the tuning re-timing errors:

1. Identify the largest passing window (LPW).
2. Selects the optimum tuning value (OTV) from LPW.
3. Locate the re-timing tuning error using step size = 1.
4. Move away from the re-timing tuning error.

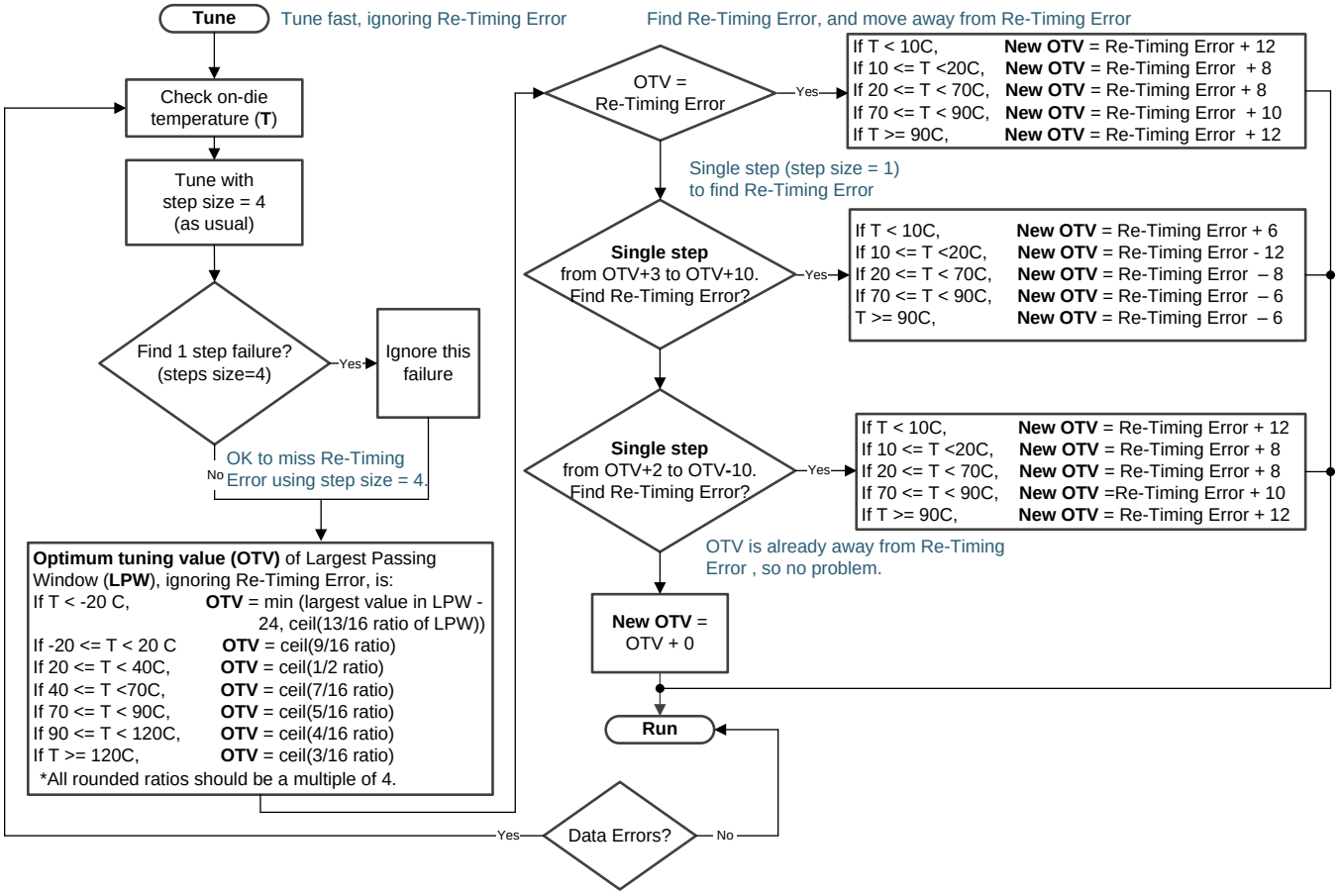

Figure 6. Tuning Algorithm Flow Chart

(1) Legacy MMC DLL tuning algorithm are algorithms that were implemented before errata i929 was published. These algorithms do not take temperature nor single step tuning into consideration and were only tuned with step size = 4.

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Diagram logic is explained as follows:

1. Identify the largest passing window (LPW). The software begins with the regular tuning algorithm using 4-steps increments to optimize boot time. At this stage, the tuning re-timing error is ignored; it will be located later.
2. Select optimum tuning value (OTV) from LPW. Choose ratio with margin. the software reads the on-die temperature sensor to determine operating condition. Band errors 1 and 2 shift to a larger value when temperature increases, so at different temperature a different ratio will yield the most margin.
    1. At low temperature, choose a larger tuning ratio (for example, 13/16th)
    2. At high temperature, choose a smaller tuning ratio (for example, 1/2)

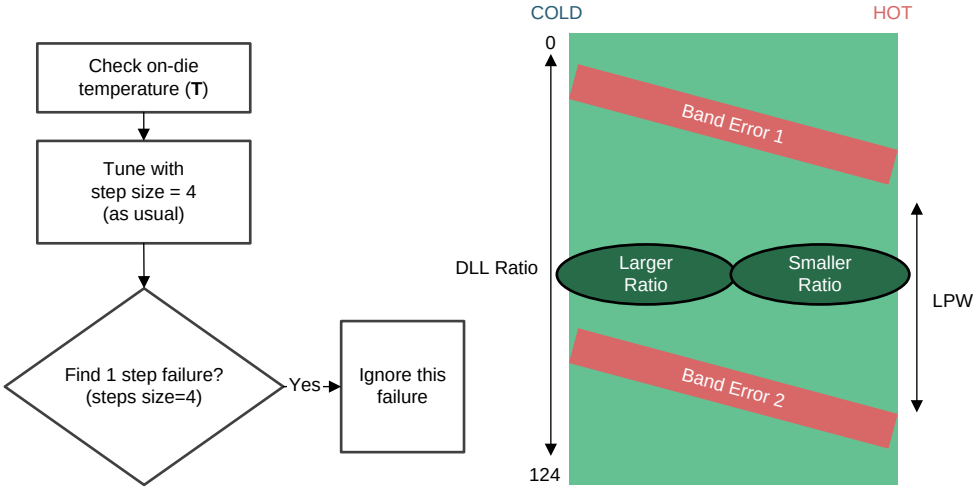

Figure 7. Flow Chart Explained (Steps 1-2)

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Both tuning band errors and tuning re-timing errors shift with temperature. To accommodate for this dependency, multiple OTV ratios were defined depending on the on-die temperature.

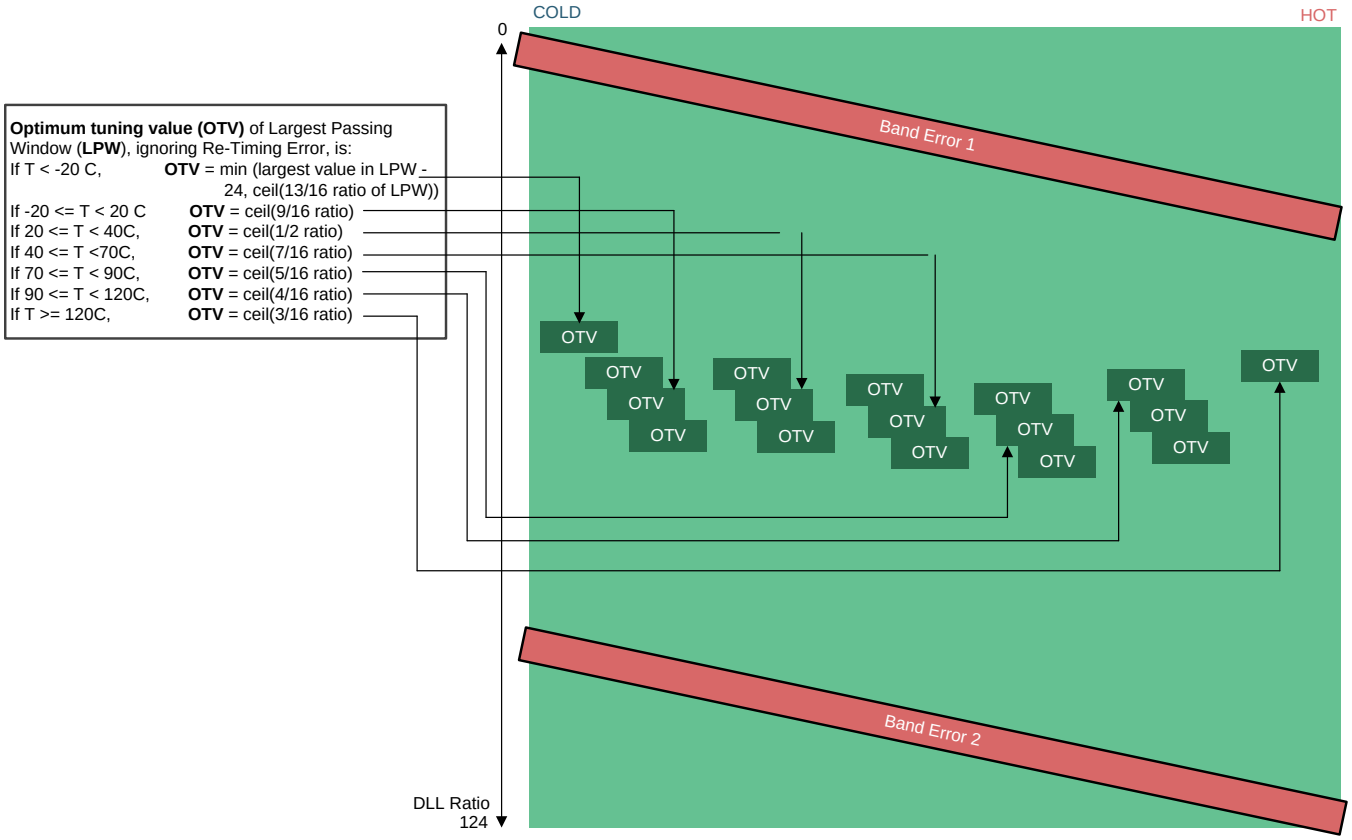

Figure 8. Flow Chart Explained (Steps 1-2)

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3. Locate re-timing tuning error in step size = 1. Once the initial ratio is chosen within the largest passing window, the software will check 10 tuning steps in each direction, using single steps, to identify whether the chosen ratio is at risk of a tuning re-timing error. The re-timing error shifts by <= +10 steps from low to high temp, so searching 20 steps around OTV will guarantee re-timing error can be located if it will impact OTV functionality. If at risk, then the value of the chosen ratio will be adjusted to move away from the error. If not, then the chosen ratio will be used unchanged.

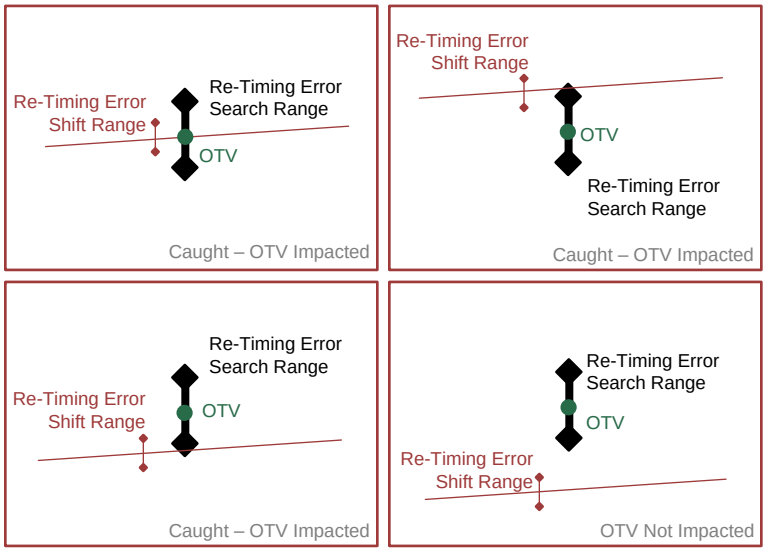

Figure 9. Flow Chart Explained (Step 3)

4. Move away from re-timing tuning error. Both tuning re-timing error and band errors 1 and 2 have a dependency on temperature. Tuning re-timing error shifts to a smaller value when temperature increases; band errors, on the other hand, shifts to a larger value. Taking these two dependencies into consideration, the initial location of re-timing error in relation to OTV is vital to move away from re-timing error without trading off performance
   1. If the re-timing error is a larger ratio than OTV, the smaller ratio offers more margin from both band errors and re-timing error. Move away from re-timing error by choosing a smaller ratio as the final OTV. NOTE: The situation is different in cold temp because re-timing error is at the largest value at this point. Hence, choose a larger ratio for cold temp ONLY.

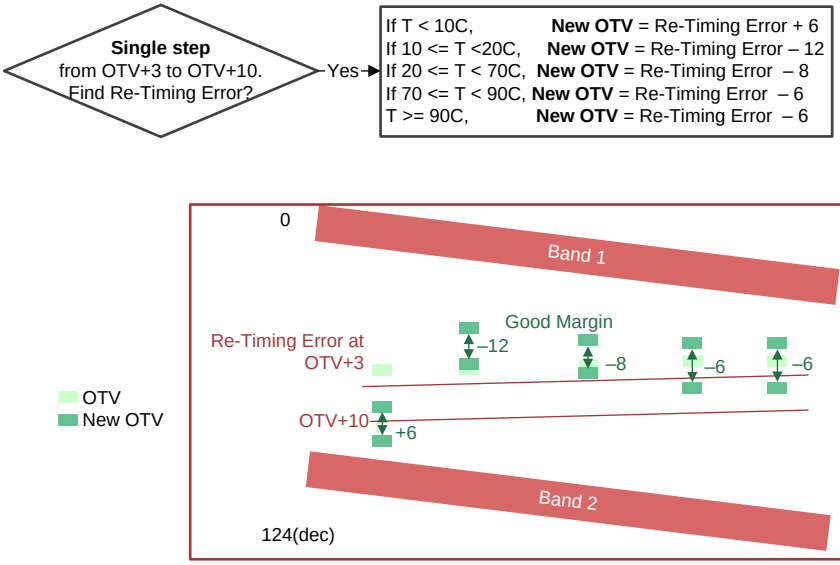

Figure 10. Flow Chart Explained (Steps 4)

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2. If the re-timing error is a smaller ratio than OTV, the large ratio offers more margin from both band errors and re-timing error. Move away from re-timing error by choosing a larger ratio as the final OTV.

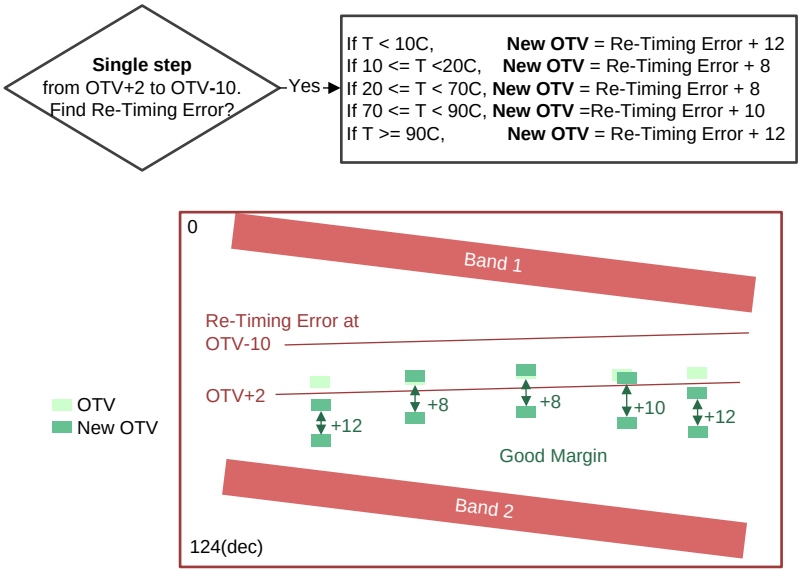

Figure 11. Flow Chart Explained (Step 4)

3. If the re-timing error is not found within 20 steps of OTV, OTV is not impacted by this errata and the value is safe to use for functionality.

4 Board Designs

Customers may tailor their boards to ensure center ratio of the largest passing window never fall near the expected failing range. This can be done by reviewing MMC output timing data, and route the MMC signal traces accordingly.

5 FAQs

- **Question:** Will the re-timing error always be caught?

  Answer: Yes, the re-timing error is always caught using step size = 1. The second stage latch in the MMC DLL has a min setup or hold time requirement of at least one DLL tap.
- **Question:** Why does the re-timing error shift to a smaller ratio at higher temperatures?

  Answer: The System-on-Chip (SoC) transistors perform slower when the temperature increases, which results in a smaller number of ratios needed to delay the CLK by a full clock cycle.
- **Question:** Why does the band error shift to a larger ratio at higher temperatures?

  Answer: The band errors are related to slave MMC memory output timings.
- **Question:** How do customers determine the chosen ratio of DLL?

  Answer: Customers can read the MMCHS_DLL[19:13] FORCE_SR_C field after tuning to determine the chosen ratio for DLL.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2018) to B Revision	Page
• Update was made in Section 2.1.	4
• Update was made in Section 5	8

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