EVM User's Guide: DP83826-EVM-AM2

DP83826-EVM-AM2 User Guide

Description

DP83826-EVM-AM2 is an Industrial Ethernet PHY add-on board to be used with AM2x series Sitara™ high-performance microcontroller evaluation modules. This add-on board is an excellent choice for initial Ethernet evaluation and prototyping using AM2x EVMs. DP83826-EVM-AM2 is equipped with a TI DP83826 low latency 10/100-Mbps PHY with MII interface and enhanced mode, and a standard RJ45 Ethernet networking connector. DP83826-EVM-AM2 is currently supported on TMDSCNCD263P and the AM263Px MCU PLUS SDK.

Features

The Sitara™ AM2x EVM Industrial Ethernet PHY Add-on Board has the following features:

- DP83826 low latency 10/100-Mbps Industrial Ethernet PHY with MII interface and enhanced mode
- Standard RJ45 Ethernet networking connector
- Shielded DF40GB 48-pin connector for interfacing with Sitara™ AM2x series evaluation modules

1 Evaluation Module Overview

Preface: Read This First

1.1 Sitara MCU+ Academy

Texas Instruments offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.2 If You Need Assistance

If you have any feedback or questions, support for the Sitara AM2x MCUs and the AM2x EVM Industrial Ethernet PHY Add-on Board development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in Section 5.1.

1.1 Introduction

The AM2x EVM Industrial Ethernet PHY Add-on Board was developed to enable additional Ethernet peripheral support on AM2x EVMs and allow for rapid prototyping of the core SoC for Industrial Ethernet applications. This User Guide details the design of the add-on board and how to properly use the interface. The User Guide also details many important aspects of the board including, but not limited to pin header descriptions, test points, and signal routing.

1.2 Kit Contents

The Sitara AM2x EVM Industrial Ethernet PHY Add-on Board kit contains the following items:

- DP83826-EVM-AM2 Industrial Ethernet PHY Add-on Board

Not included:

- Sitara AM2x EVM

Note

DP83826-EVM-AM2 can be available as a virtual bundle with select Sitara AM2x EVMs. Visit the EVM product page (DP83826-EVM-AM2) for more information.

1.3 Device Information

The DP83826 offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems.

The two configurable modes are BASIC standard Ethernet mode that uses a common Ethernet pinout, and ENHANCED Ethernet mode which supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with the additional features and hardware bootstraps configuration.

For additional information, refer to the DP83826 data sheet.

2 Hardware

2.1 Component Identification

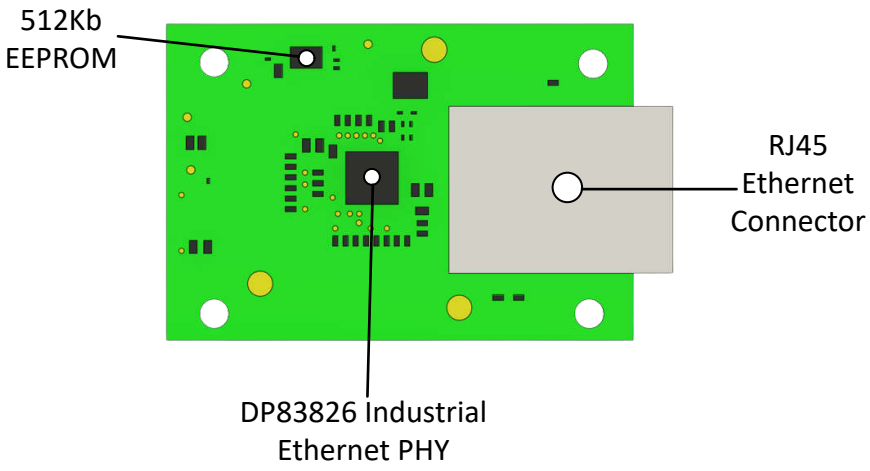


Figure 2-1. DP83826-EVM-AM2 Top Side

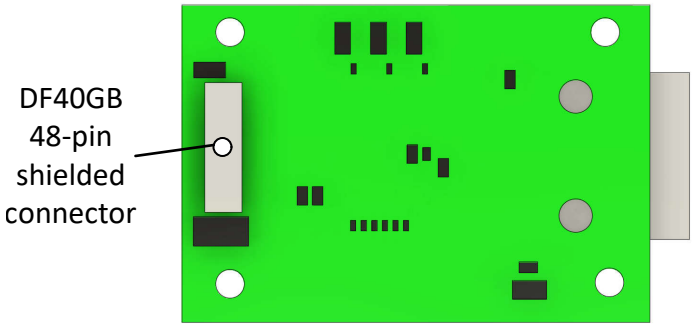


Figure 2-2. DP83826-EVM-AM2 Bottom Side

2.2 Power Requirements

The AM2x EVM Industrial Ethernet PHY Add-on Board is powered from a 3.3V input from the DF40GB 48-pin connector that interfaces the DP83826-EVM-AM2 with the main MCU EVM. The following sections describe the power distribution network topology that supply the AM2x EVM Industrial Ethernet PHY Add-on Board, supporting components, and reference voltages.

2.2.1 Power Tree

The DP83826-EVM-AM2 power is supplied from the main Sitara AM2x EVM via the DF40GB connector.

3.3V (VDDIO) is connected to pin 44 and 46 on the DF40GB connector, and is passed to the source inputs on the DP83826ERHBT Industrial Ethernet PHY through a pair of ferrite beads (one per supply net).

Figure 2-3 shows the power connections of DP83826-EVM-AM2.

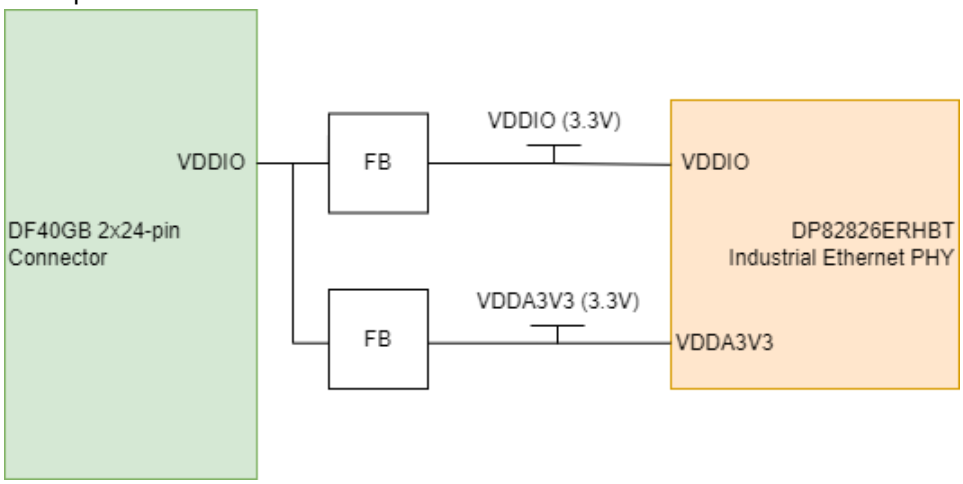


Figure 2-3. Power Tree

2.3 Functional Block Diagram

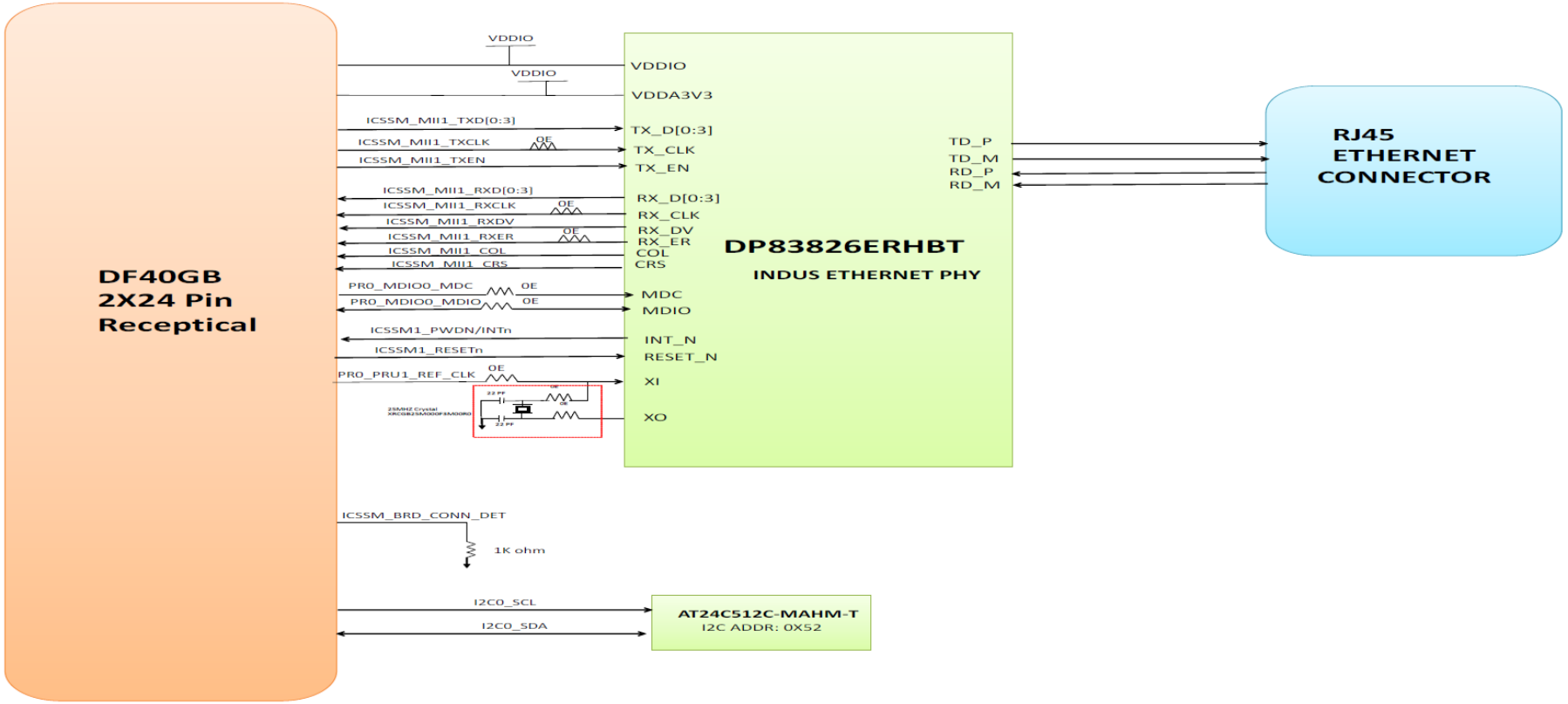


Figure 2-4. AM2x Industrial Ethernet PHY Add-on Board Block Diagram

2.4 Header Information

The DP83826-EVM-AM2 is equipped with a Hirose DF40GB 2x24-pin connector (J2) to connect to Sitara AM2x EVMs. Listed below are the features of this connector relevant to this EVM:

- 2x24 pins
- Shielded type to support high-speed signals and prevent noise
- High density mounting

Refer to Table 2-1 for a complete list of the header pins and descriptions.

Table 2-1. DF40GB Header Pinout

Pin #	Signal	Description		Description	Signal	Pin #
1	GND	Ground		PMIC External Voltage Monitor	EXT_VMON2	2
3	TX_CLK	Transmit Clock		2.5V supply	VDD_2V5	4
5	GND	Ground		2.5V supply	VDD_2V5	6
7	TX_D0	Transmit Data 0		Ground	GND	8
9	TX_D1	Transmit Data 1		Interrupt To Ethernet PHY	PWDN/INTn	10
11	TX_D2	Transmit Data 2		Reset input to Ethernet PHY	RESETn	12
13	TX_D3	Transmit Data 3		Collision Detected	COL	14
15	GND	Ground		Ground	GND	16
17	GND	Ground		Ground	GND	18
19	RX_CLK	Receive Clock		MDIO Clock	MDIO_MDC	20
21	GND	Ground		MDIO Data	MDIO_MDIO	22
23	RX_D0	Receive Data 0		Ground	GND	24
25	RX_D1	Receive Data 1		Inhibit	INH	26
27	RX_D2	Receive Data 2		PRUx Reference Clock	REF_CLK	28
29	RX_D3	Receive Data 3		Carrier Sense	CRS	30
31	GND	Ground		Ground	GND	32
33	GND	Ground		Ground	GND	34
35	TXEN	Transmit Enable		Board Connection Detect	BRD_CONN_DET	36
37	EEPROM_A2	EEPROM I2C Address bit [2]		IEEE 1588 SFD	1588_SFD	38
39	RX_ER	Receive Data Error		I2C Clock	I2C_SCL	40
41	GND	Ground		I2C Data	I2C_SDA	42
43	RX_LINK	Receive Indicator		IO Voltage Supply	VDDIO	44
45	RXDV	Receive Data Valid		IO Voltage Supply	VDDIO	46
47	EEPROM_A0	EEPROM I2C Address bit [0]		Audio Bit Clock	GPIO_2/CLKOUT	48

2.5 Test Points

DP83826-EVM-AM2 is equipped with multiple test points for hardware debug and bench testing. Table 2-2 shows the test points on the board and their associated signal net.

Table 2-2. DP83826-EVM-AM2 Test Points

Test Point	Signal	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	GND	Ground
TP4	GND	Ground
TP5	RXDV	Receive Data Valid
TP6	RXD0	Receive Data 0
TP7	RXD1	Receive Data 1
TP8	RXD2	Receive Data 2
TP9	RXD3	Receive Data 3
TP10	MDIO_MDC	MDIO Clock
TP11	MDIO_MDIO	MDIO Data
TP12	RXCLK	Receive Clock
TP13	1588_SFD	IEEE 1588 SFD
TP14	RXER	Receive Data Error
TP15	INH	Inhibit
TP16	TXEN	Transmit Enable
TP17	TXCLK	Transmit Clock
TP18	TXD0	Transmit Data 0
TP19	TXD2	Transmit Data 2
TP20	TXD1	Transmit Data 1
TP21	TXD3	Transmit Data 3
TP22	CRS	Carrier Sense
TP23	COL	Collision Detected
TP24	RXLINK	Receive Indicator
TP25	EXT_VMON	PMIC External Voltage Monitor
TP26	GND	Ground
TP27	GND	Ground

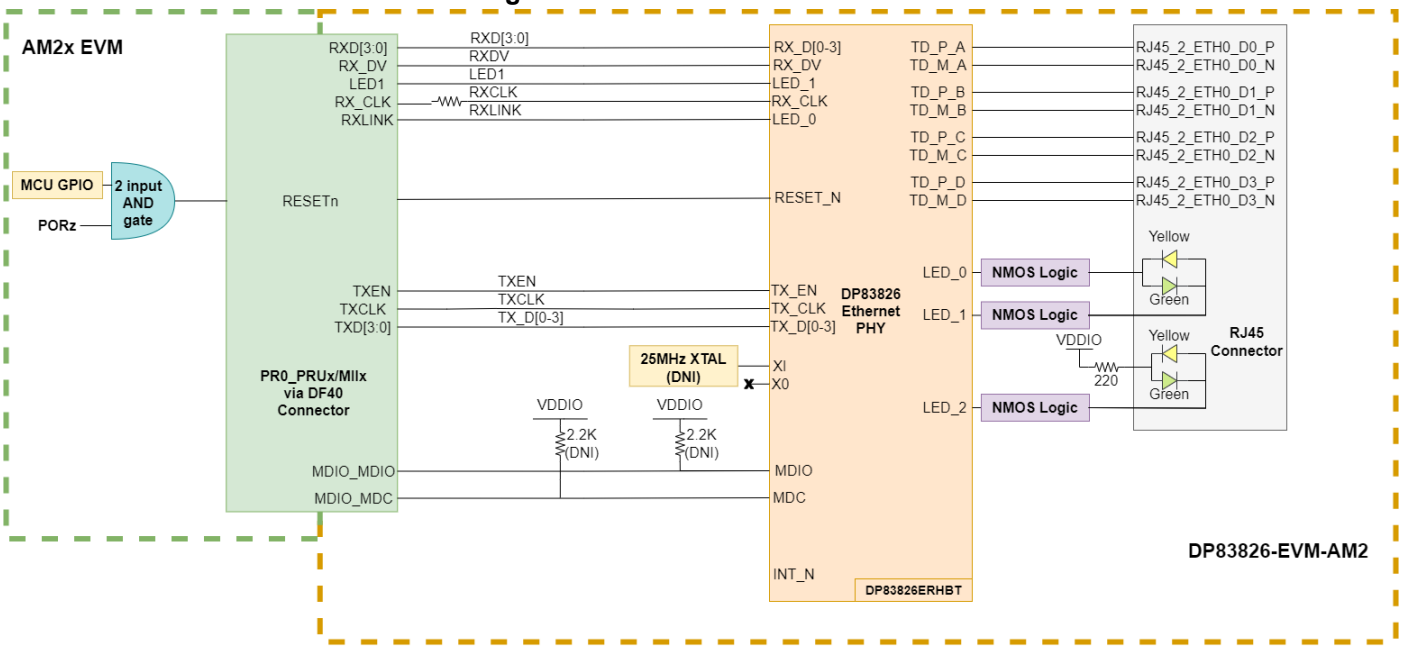
2.6 Interfaces

2.6.1 Ethernet Interface

2.6.1.1 Industrial Ethernet PHY

The AM2x EVM Industrial Ethernet PHY Add-on Board uses one port of RGMII signals and the PRUx core of the PRU-ICSS to be connected to a 32-pin Ethernet PHY (DP83826ERHBT). The PHY is configured to advertise 10/100 Mb operation. The Ethernet data signals of the PHY are terminated to an RJ45 Connector. LEDs are used to indicate link status and activity.

Figure 2-5. Industrial Ethernet PHY



The Ethernet PHY requires two power sources, VDDIO (3.3V or 1.8V) and VDDA3V3 (3.3V) which are supplied through the DF40GB connector (J2).

On some AM2x EVMs, the RGMII port of the CPSW signals are internally muxed on the same balls of the MCU as the PRU-ICSS ethernet signals. To use RGMII, the balls must be set to the appropriate mux mode for RGMII.

The MDIO and Interrupt signals from the main EVM SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. These resistors are not assembled by default on the DP83826-EVM-AM2, but there are footprints if the main EVM does not have these signals pulled up. The interrupt signal is driven by a GPIO signal that is mapped from the main EVM SoC.

The reset signal for the Ethernet PHY is most often driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the main SoC EVM and a power-on reset signal on the main EVM.

2.6.1.2 Industrial Ethernet PHY Strapping Resistors

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

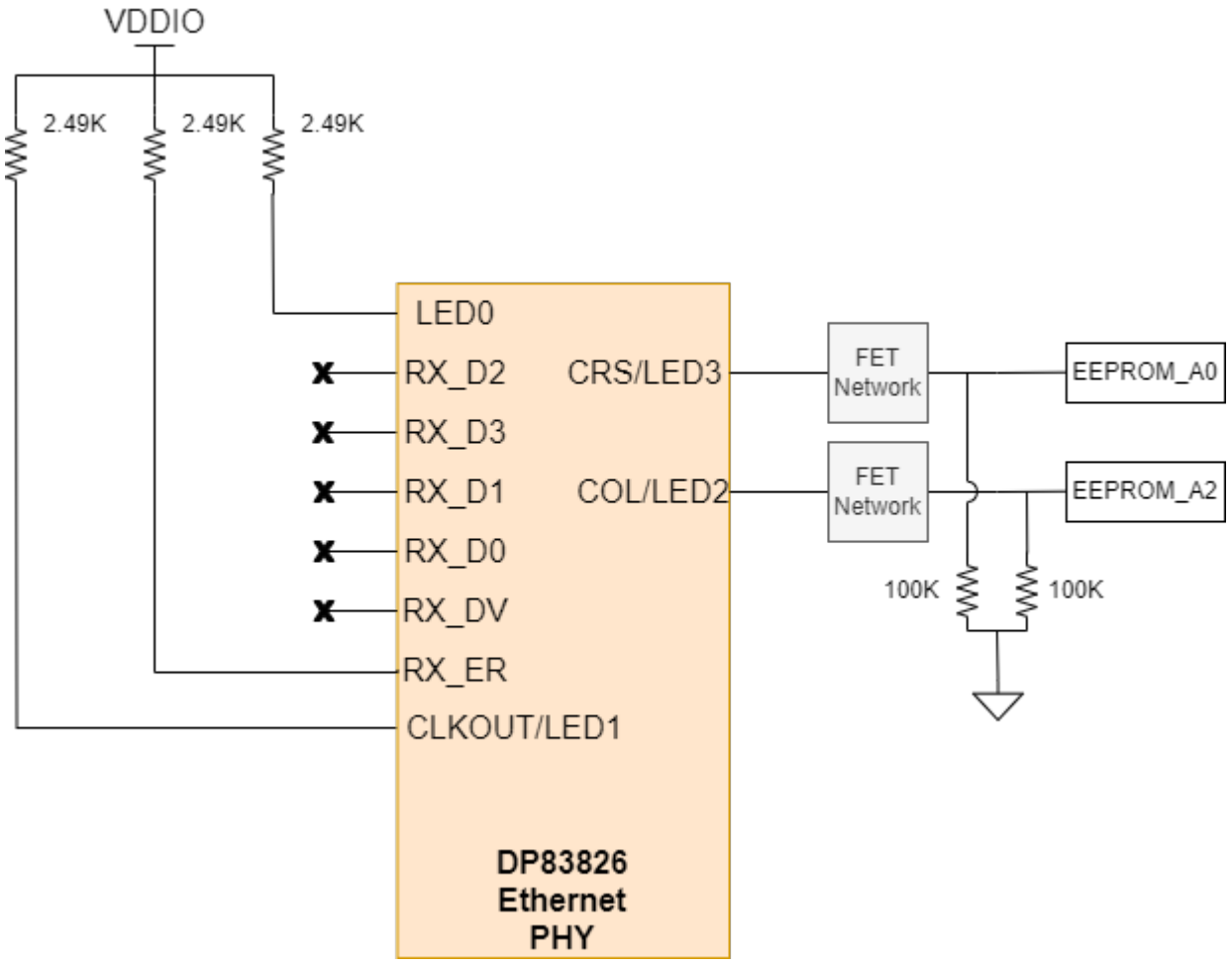


Figure 2-6. Industrial Ethernet PHY Strapping Resistors

Table 2-3. Industrial 10/100 Mbit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode on DP83826-EVM-AM2	Function
LED0	0	1	PHY address: 3b[EEPROM_A2][EEPROM_A0]1. See Section 2.6.1.4 for more information on PHY addressing.
CRS/LED3	0	EEPROM_A2	
COL/LED2	0	EEPROM_A0	
RX_D2	0	0	MII MAC Mode
RX_D3	0	0	Fast link-drop disable
RX_D1	0	0	auto MDIX enable
RX_D0	0	0	auto-negotiation enable
RX_DV	0	0	
RX_ER	0	1	LED1 on PHY Pin 31
CLKOUT/LED1	1	1	Odd nibble detection enabled

2.6.1.3 LED Indication in RJ45 Connector

The AM2x EVM Industrial Ethernet PHY Add-on Board has one RJ45 network ports for the ICSSM port on PRU0 of the main EVM SoC. The RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

- RJ45 Connector LED indication for the ICSSM PRU0 port:

Table 2-4. ICSSM PRU1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	10BT speed link is up
Left LED	Green	Link OK
	Yellow	1000BT speed link is up

2.6.1.4 Multi-Connector Addressing

For Sitara AM2x EVMs with more than one Ethernet add-on board connector, each DP83826-EVM-AM2 requires a different EEPROM I2C address and PHY address. The EEPROM A0 and A2 nets, set by pull resistors on the main Sitara AM2x EVM drive the PHY address nets via a FET network implemented on the DP83826-EVM-AM2. Table 2-5 details the multi-connector I2C and PHY addressing scheme implemented on the add-on PHY board.

Note

- The EEPROM I2C address bits A2 and A0 are driven via pull resistors on the main Sitara AM2x EVM. The pull resistors for each enumerated connector follow the table below.
- EEPROM I2C address bit A1 will **always** be pulled high to VDDIO on the add-on board
- The EEPROM I2C address is defined by the following 8 bits: 8b1010[A2][A1][A0][R/W]
- Pulls to VDDIO/GND are via 10kOhm resistor
- All EVMs with a single connector are configured as CONNECTOR_0

Table 2-5. Multi-Connector I2C / PHY Addressing Scheme

Connector_#	EEPROM_A2 (connector pin 37)		EEPROM_A1		EEPROM_A0 (connector pin 47)		I2C Address	DP83826 PHY Address
	Pull	A2	Pull	A1	Pull	A0		
CONNECTOR_0	GND	0	VDDIO	1	GND	0	0x52	3b001
CONNECTOR_1	GND	0	VDDIO	1	VDDIO	1	0x53	3b011
CONNECTOR_2	VDDIO	1	VDDIO	1	GND	0	0x56	3b101
CONNECTOR_3	VDDIO	1	VDDIO	1	VDDIO	1	0x57	3b111

2.7 Integration Guide

The Sitara AM2x Ethernet Add-on Board ecosystem is not limited to the DP83826x Industrial Ethernet PHY. A wide variety of Industrial Ethernet PHYs with Sitara AM2x MCU compatible signals can be designed onto add-on boards to be used across Sitara AM2x MCU EVMs. This section details the mechanical information and provide the necessary dimensions for designing an Industrial Ethernet PHY add-on board.

Note

All dimensions are measured in inches.

2.7.1 Board Dimensions

Figure 2-7 shows the proper PCB dimensions for an Industrial Ethernet PHY add-on board to be compatible with Sitara AM2x EVMs.

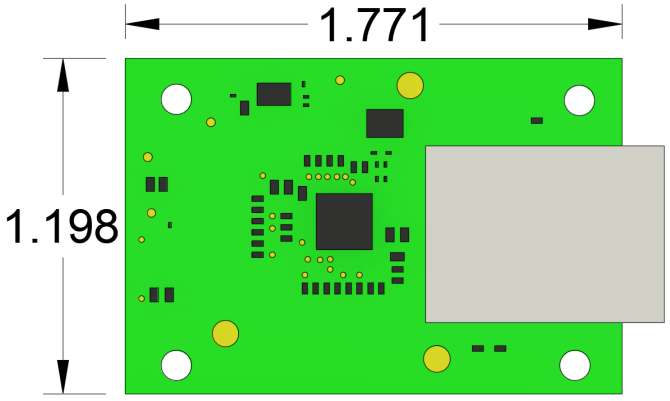


Figure 2-7. Industrial Ethernet PHY Add-on Board Dimensions

Figure 2-8 shows the side profile of the PCB.

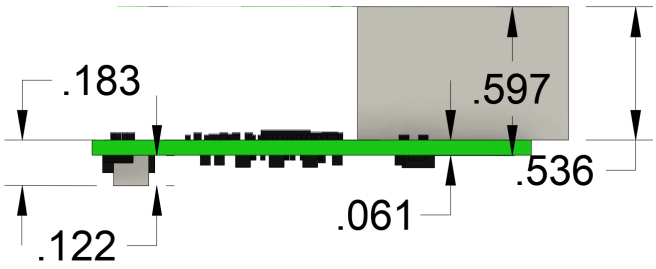


Figure 2-8. Industrial Ethernet PHY Add-on Board Side Profile

2.7.2 DF40GB Connector

TI recommends the 48-pin (2x24) Hirose DF40GB high-density, shielded connector for Ethernet PHY Add-on Boards interfacing with Sitara AM2x EVMs. Figure 2-9 shows the mounting position of the DF40GB connector on the DP83826-EVM-AM2.

The origin of the connector is to be placed at **(x,y)=(0.157,0.537)**.

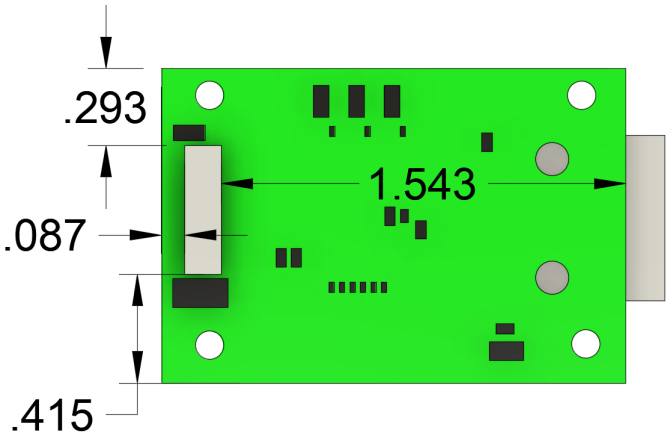


Figure 2-9. DF40GB Connector Mounting Position

2.7.3 Mounting Holes

The DP83826-EVM-AM2 is designed with mounting holes to securely attach to the main Sitara AM2x MCU EVM. The compatible Sitara AM2x EVMs are designed to have matching mounting holes for an Ethernet Add-on Board to connect to. Screws and spacers can be inserted into the mounting holes for a more permanent configuration. Figure 2-10 shows the positions of the mounting holes on the DP83826-EVM-AM2.

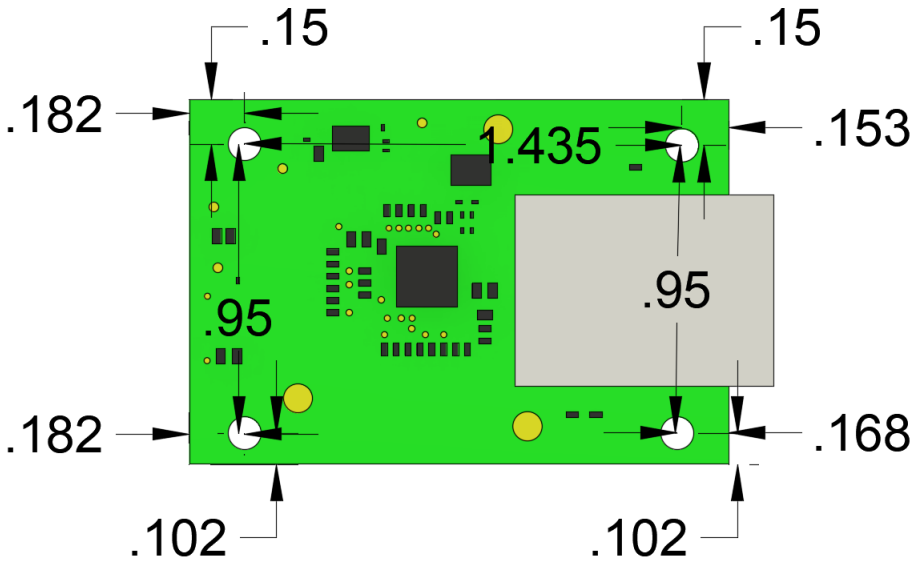


Figure 2-10. Mounting Hole Positions

2.7.4 RJ45 Ethernet Connector

The DP83826-EVM-AM2 has an RJ45 Ethernet Connector for sending and receiving signals from the DP83826 Ethernet PHY. Different Industrial Ethernet PHYs utilize the same connector, and must be used on custom Industrial Ethernet PHY Add-on Boards. Figure 2-11 shows the position of the RJ45 connector on the DP83826-EVM-AM2.

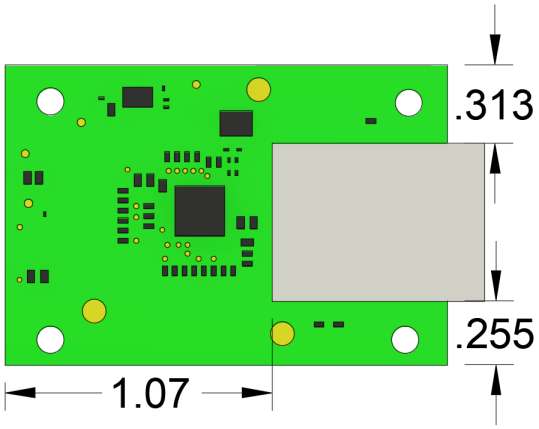


Figure 2-11. RJ45 Connector Position

3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, go to the EVM product page on ti.com (DP83826-EVM-AM2).

4 Additional Information

4.1 Trademarks

Sitara™ and E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM263P controlCARD Evaluation Module Tool Folder*
- *AM263P controlCARD Evaluation Module User's Guide*
- *Texas Instruments Code Composer Studio*

5.2 Compatible Sitara™ MCU AM2x EVMs

This Ethernet add-on board is compatible with the following EVMs:

- *TMDSCNCD263P*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 1, 2024 to September 30, 2024 (from Revision * (January 2024) to Revision A (September 2024))	Page
• [Header Information] Updated DF40GB header pinout to match Rev A design	6
• [Test Points] updated TP list for Rev A design	7

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