Technical Article

How to latch off a power converter that has a hiccup fault response

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Power converters are typically designed to protect against unwanted fault scenarios. For example, if too much current is being drawn on the converter output, overcurrent protection may engage. This is helpful if the converter's output terminals are accidentally shorted together or if the load current goes above the designed maximum current. Other common fault situations include exceeding the thermal shutdown trip point (overheating) and the output voltage going out of bounds (overvoltage or undervoltage).

A popular way to respond to faults is called a hiccup. The power converter will turn itself off, wait for some time (30 ms, for example) and then automatically restart itself. Figure 1 shows an example of this response, measuring both the output voltage and inductor current. A hiccup fault response gives the system a chance to recover without external intervention. It also helps reduce the power consumed and heat generated in the case of shorted outputs.

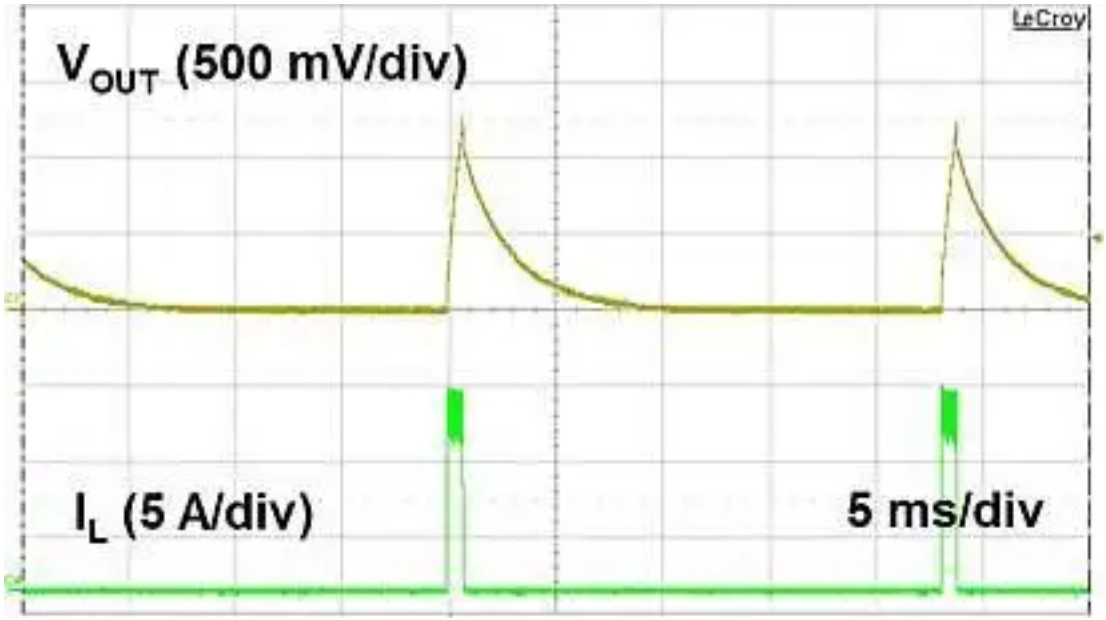
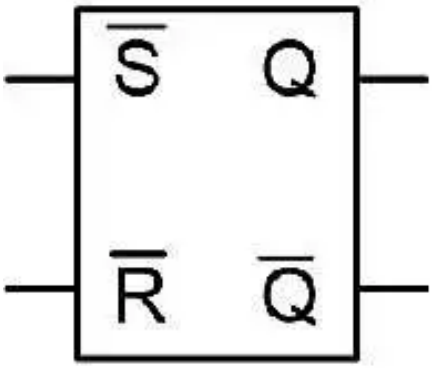


Figure 1. Hiccup fault response caused by an overcurrent scenario.

There are times when a hiccup response is not wanted. Perhaps you want a central controller to manage the fault response in a more complex or sophisticated manner. Some systems have redundancy built in and want to completely turn off the faulting subsystems in order to ensure that they do not interfere with functioning subsystems. In these cases, the desired fault response may be to latch off the faulting power converters. Latching off the power converter will prevent it from restarting unless the enable (EN) pin or supply voltage is cycled to reset the latch. Some devices, like the TPS53511, have a built-in latch-off response, but most do not.

It is possible to add a latch-off fault response to a power converter with a simple set/reset (SR) latch circuit. Figure 2 shows an SR latch and its truth table. For this example, the SR latch has active-low inputs. This means that when the inputs are high, the outputs Q and Q-Bar do not change. If the set input goes low, Q will be set high (1). If reset goes low, Q will be low (0). If both inputs are low, the outputs are in an undetermined state, a situation that generally should be avoided. Additional logic gates can overcome this situation.



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	X	X

Figure 2. SR latch with active-low inputs and corresponding truth table.

Figure 2 illustrates a high-level approach to implementing the latch circuit. Many power converters and monitoring circuits have a power good (PGOOD) output. If there is a fault in the converter, the PGOOD signal will pull low, indicating that the converter has a problem. When the PGOOD signal goes low, the output of the latch circuit (Q) will go high, which in turn will pull the EN pin of the converter low. The converter will turn off when the EN pin goes low and will not restart by itself. A reset signal sent to the latch restarts the converter and brings the Q output low, which in turn brings the EN pin high. The inverters are included to make interfacing simpler; they are implemented with an open-drain metal-oxide semiconductor field-effect transistor (MOSFET).

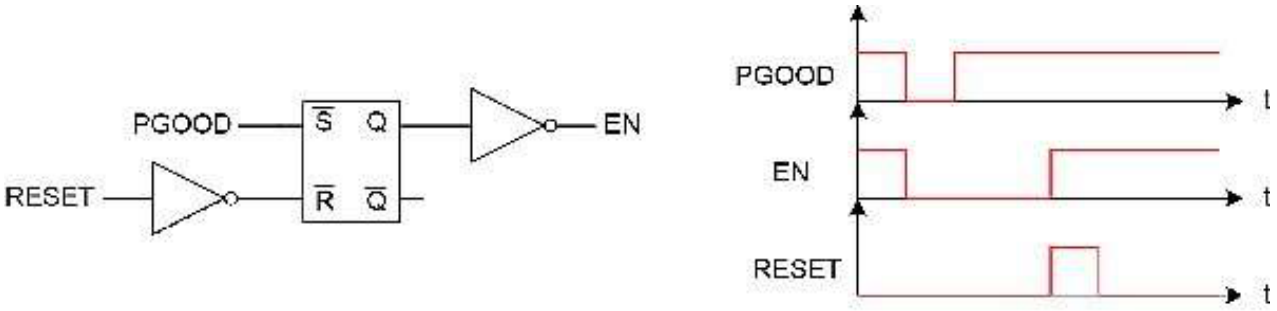
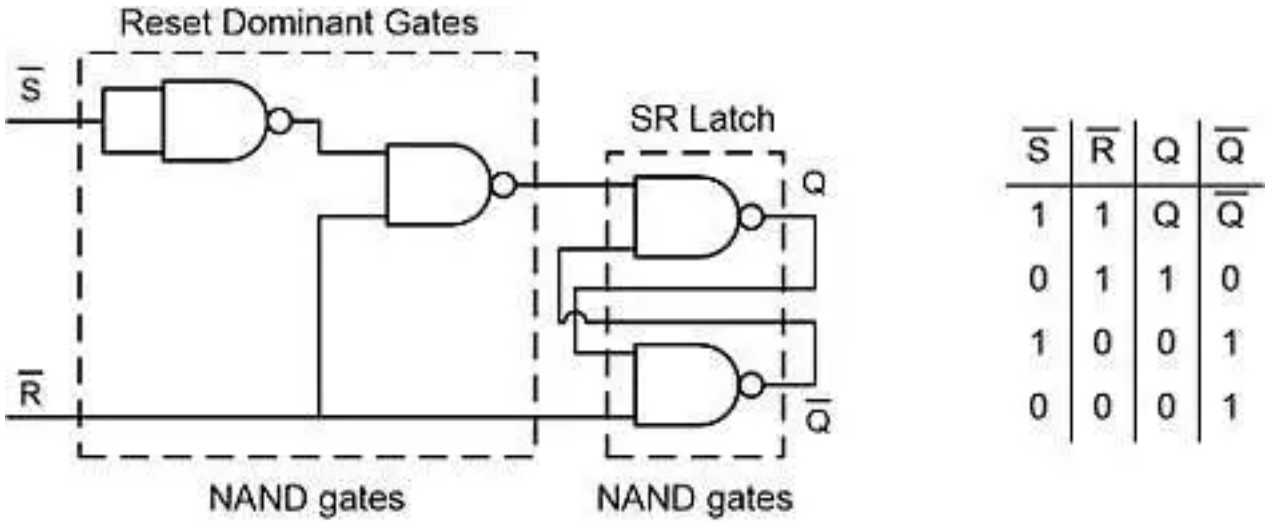


Figure 3. Latch circuit overview and example signal diagram.

You want to ensure that the converter can correctly start up or restart even while the PGOOD signal is low; thus, you need the latch circuit to be reset-dominant. In other words, when both the set and reset inputs are low, the reset input will dominate, resulting in the Q output being low. Figure 4 shows a simplified implementation using only NAND gates, with the corresponding truth table. It is possible to create this circuit with two dual NAND gate SN74AUP2G00 integrated circuits (ICs) or one quad NAND gate SN74HC00 IC.



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	0	1

Figure 4. Reset-dominant latch circuit using NAND gates and corresponding truth table.

Figure 4 shows the overall implementation of the latch-off circuit. The PGOOD pin of the power converter pulls high using an external resistor (to 3.3 V). Whenever a fault occurs, the open-drain MOSFET connected to PGOOD will pull the S-bar input to latch low. The Q output then goes high, which turns on MOSFET S1. The EN pin pulls low, which turns the converter off and prevents hiccup auto-restart. When the converter input voltage rail (PVIN) ramps up, capacitive coupling through the parasitic gate-to-drain capacitance (C_{gd}) could pull up on the gate of S1 and turn it on. A pulldown resistor on the gate of S1 may be helpful to ensure that S1 does not inadvertently turn on.

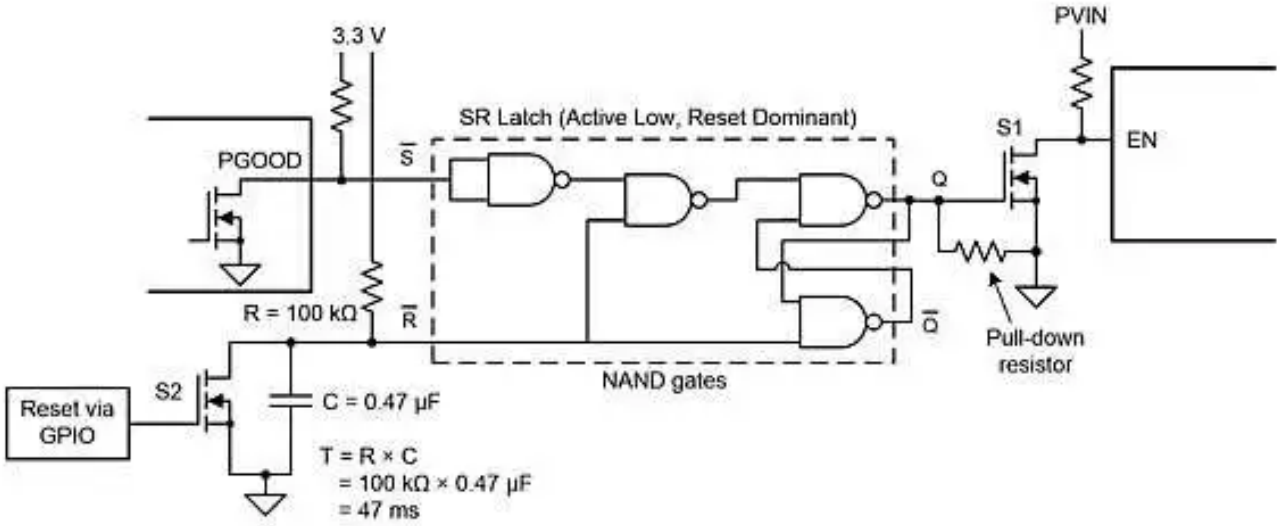


Figure 5. Resettable latch-off circuit.

The R-Bar input to the SR latch is pulled high through a 100-kΩ resistor. The open-drain MOSFET S2 can pull the R-Bar signal low whenever a reset signal is provided to the gate of S2. A capacitor (C, connected in parallel with S2) forms a delay circuit with pullup resistor R. The RC time constant of the delay is about 47 ms in this example. This delay is adjustable to ensure that the R-Bar input stays low during startup. The slow edge rate on the R-Bar can damage the inputs of the some complementary metal-oxide semiconductor (CMOS) NAND gates caused by excessive current draw. The SN74AUP2G00 gates will not be damaged by this, however, because they have relatively weak drivers.

Another approach is to either use Schmitt-trigger input NAND gates or add a Schmitt-trigger buffer at the R-Bar input. In a third option, the switch S2 can be continuously turned on to pull R-Bar low during startup, and the RC delay could be reduced or entirely removed by adjusting the R and C values.

It is possible to use the circuit described here in a wide variety of power-converter applications that require a latch-off fault response. The latch-off circuit uses a few simple components and logic gates to achieve a flexible, reliable solution.

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