TIDA-00604 Test Report
Powering the Altera® Cyclone® III with TPS65023 Power Management IC

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help **you** accelerate your time to market.

Design Resources

TIDA-00604	Design Folder
TPS65023	Product Folder
TPS65023EVM-205	Tools Folder

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center

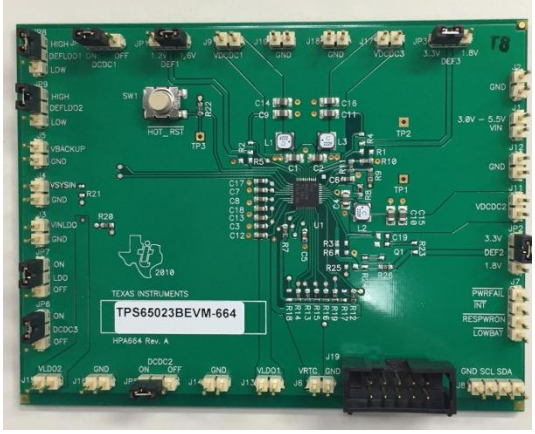


Figure 1 - Top Side

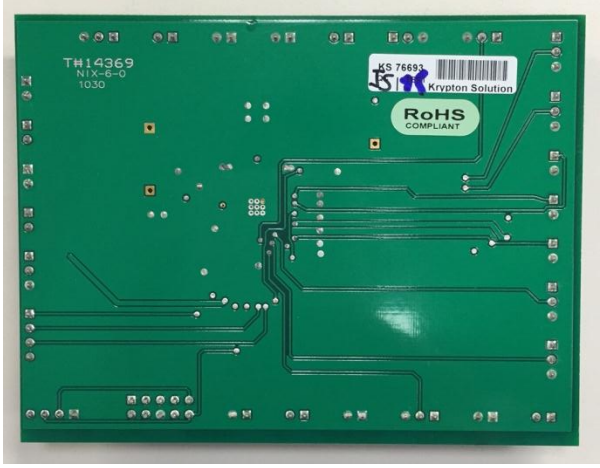


Figure 2 - Bottom Side

Report Contents

Feature Applications

- Motor Control
- Test and Measurement
- Wireless
- Motion Control
- Communication

Description

The TIDA-00604 design is a compact, integrated power solution for Altera® Cyclone® III SoC (out of the Cyclone® series family of products). This design showcases TPS65023 as an all-in-one IC used to supply the rails needed for powering the Cyclone® III SoC. The TPS65023 offers simple, flexibile output voltages and sequencing. The voltages on the DC/DC Converters can be set through software or via an external resistor divider. This power management IC has a input range from 2.5 – 6V and can be run from a single 5V supply or from a single cell Li-Ion battery. This design has been tested and verified for industrial applications (-40°C to 105°C).

TPS65023/Cyclone® III Block Diagram (Return to Top)

Power Supply Block Diagram

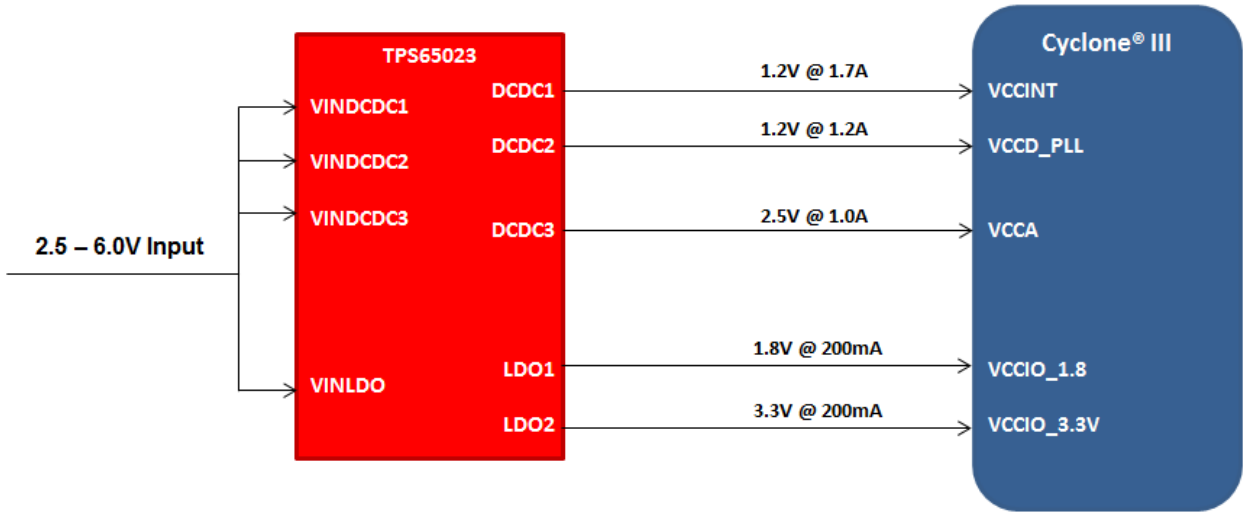


Figure 3 – Cyclone III Block Diagram

Typical Voltage and Current Requirements in End Applications

Depending on application and design on FPGA, current consumption can vary. The table below highlights the typical max currents each power output of the TPS65023 converters to the rails of the Cyclone III. The VCCIO Rails on the Cyclone III range from 1.2 – 3.3V. The TPS65023 has 2 Linear Regulators (LDOs) that can supply the full range of Cyclone III's VCCIO.

Cyclone III Supply Rails	Voltage	Supply Current (A)
VCCINT	1.2V	1.7
VCC_PLL	1.2V	1.2
VCCA	2.5V	1.0
VCCIO_1.8	1.8V	0.2
VCCIO_3.3	3.3V	0.2

Note: *The current consumption numbers above are only estimates and the actual current consumption may vary depending on the application.*

Efficiency Curves (Return to Top)

DCDC1 (Vout=1.2V) – *VCCINT*

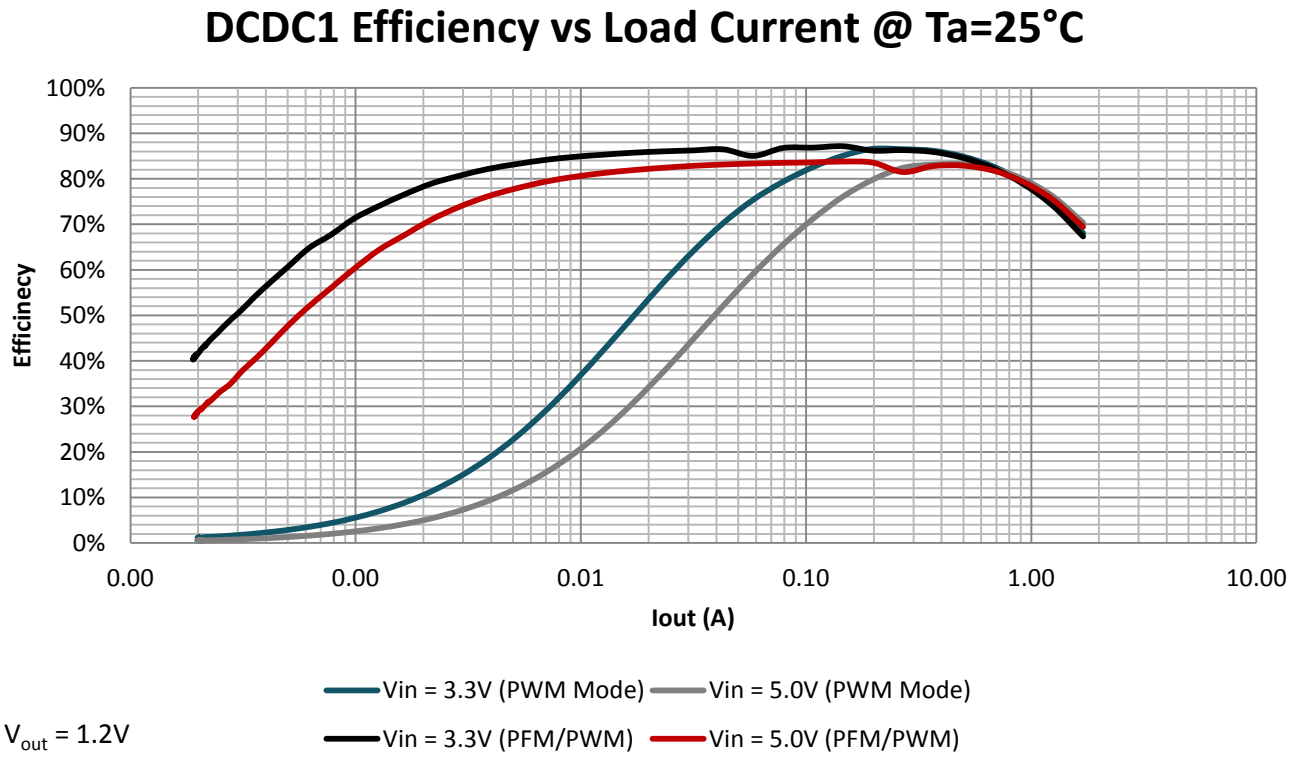
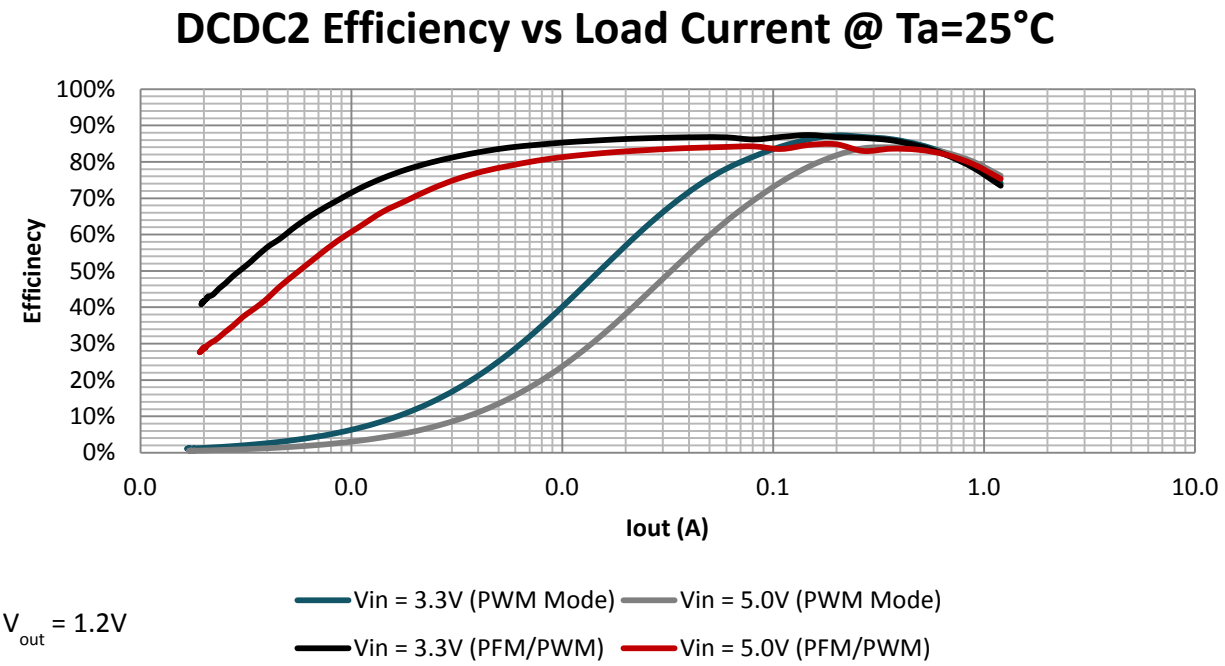


Figure 4 - DCDC1 Efficiency @ 25C

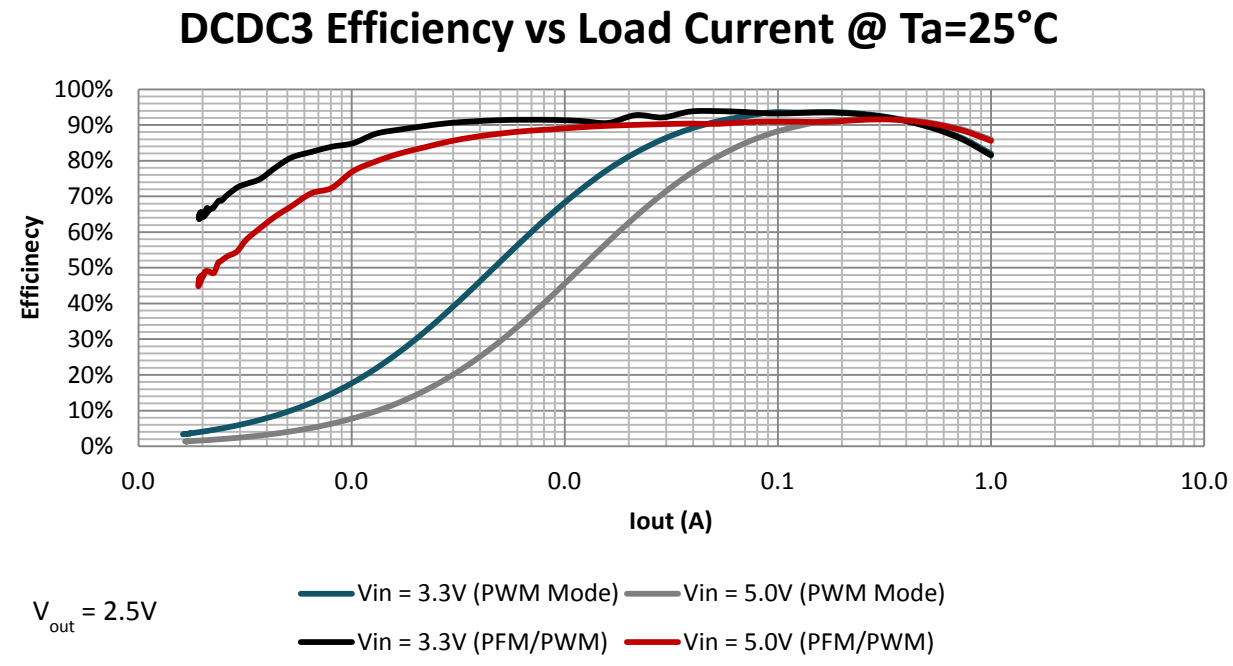
DCDC2 (Vout=1.2V) – *VCCPLL*



V_{out} = 1.2V

Figure 5 - DCDC2 Efficiency @ 25C

DCDC3 (Vout=2.5V) – *VCCA*



V_{out} = 2.5V

Figure 6 - DCDC3 Efficiency @ 25C

Load Regulation (Return to Top)

DCDC1 (Vout=1.2V) – *VCCINT*

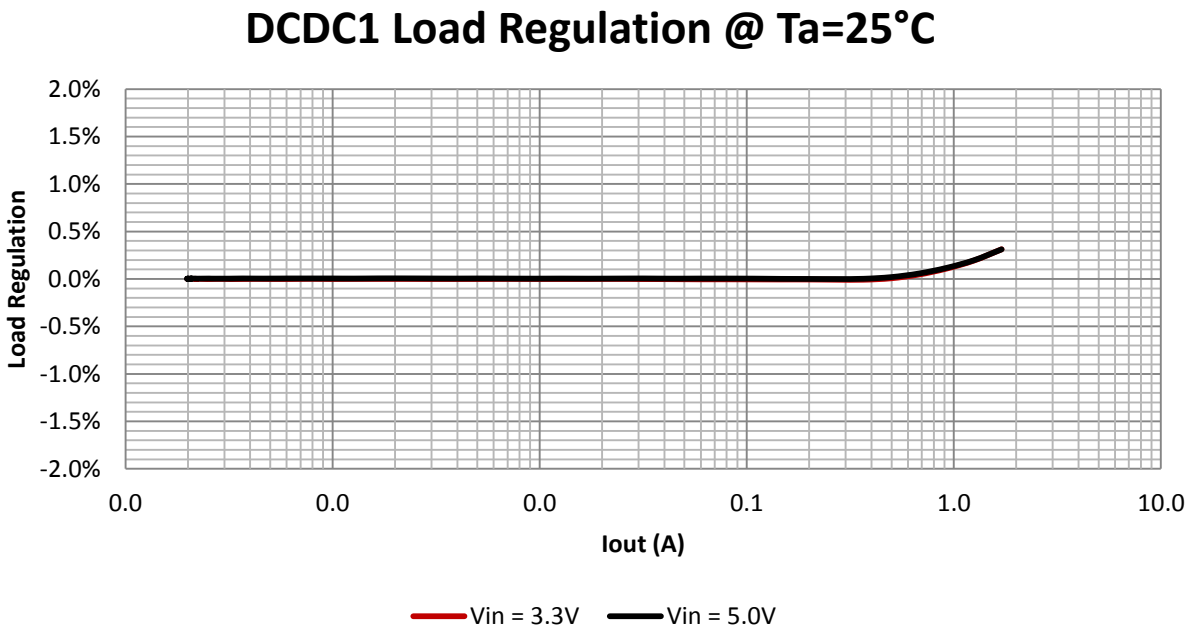


Figure 7 – DCDC1 Load Regulation @ 25C

DCDC2 (Vout=1.2V) – *VCCD_PLL*

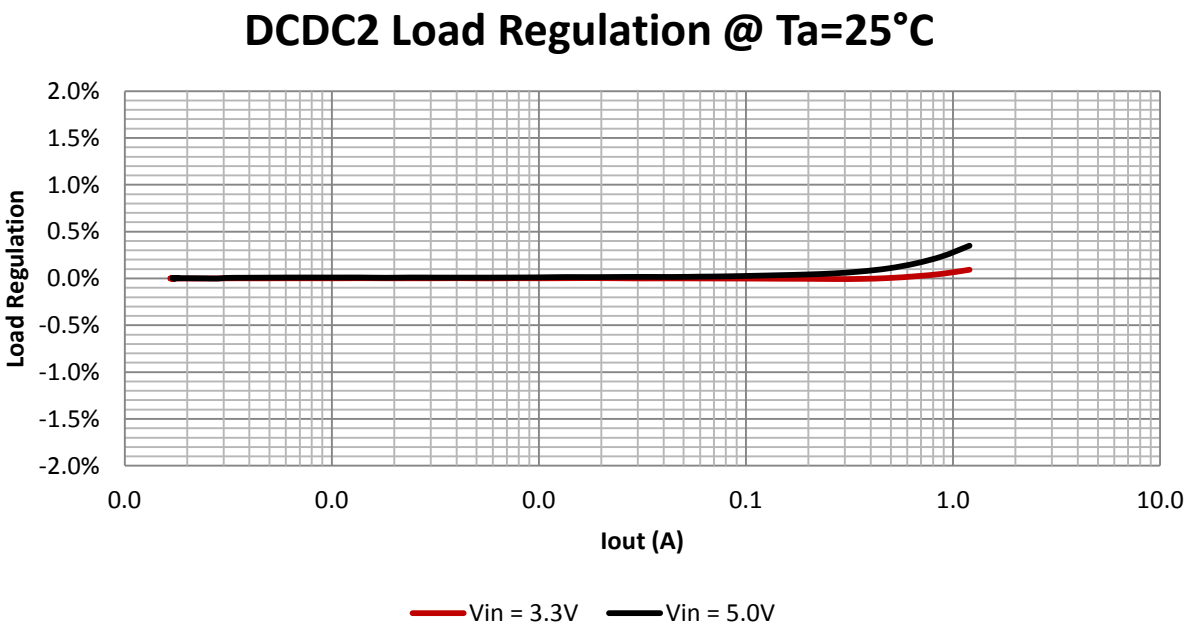


Figure 8 – DCDC2 Load Regulation @ 25C

DCDC3 (Vout=2.5V) – *VCCA*

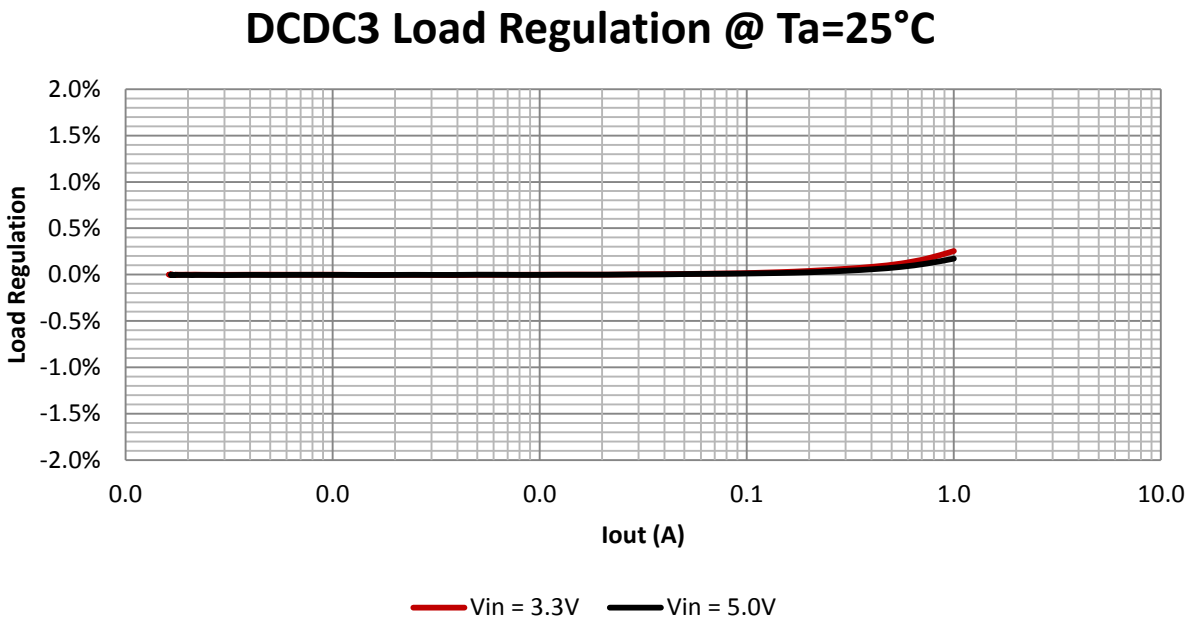


Figure 9 – DCDC3 Load Regulation @ 25C

Output Ripple Voltage (Return to Top)

DCDC1 (Vout = 1.2V) – VCCPINT (Light Load, PFM Mode)

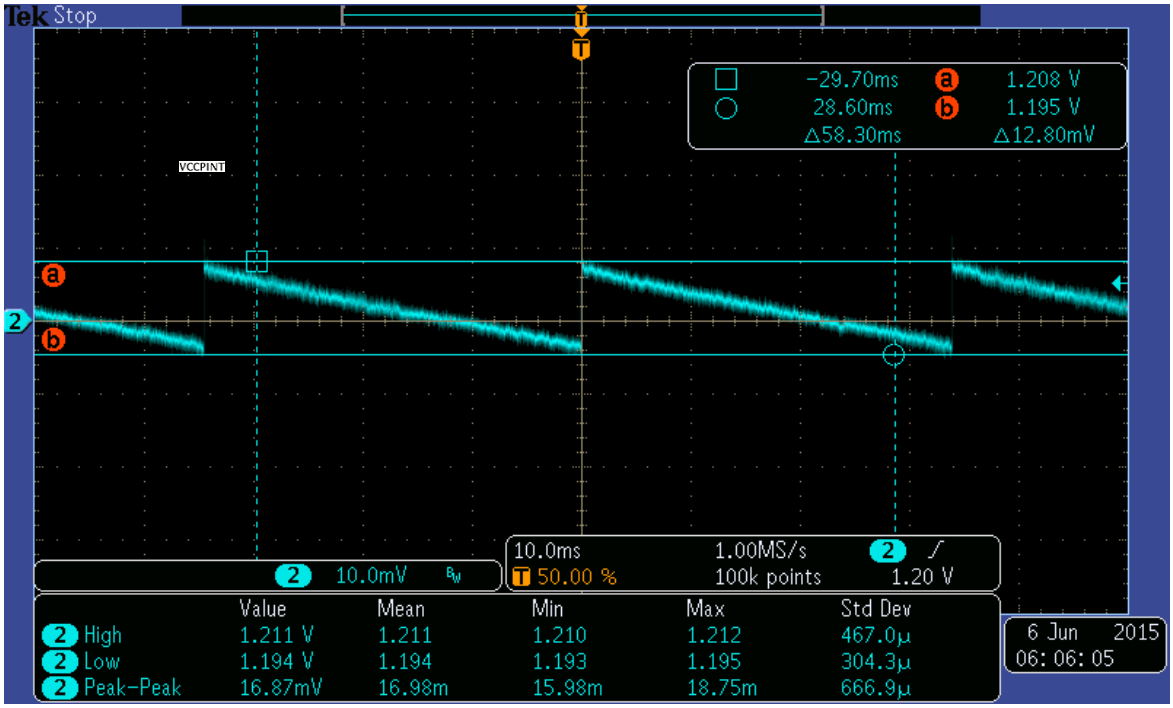


Figure 10 – DCDC1 Voltage Ripple, Light Load @ 25C

DCDC1 (Vout = 1.2V) – VCCPINT (Max Typical Load)

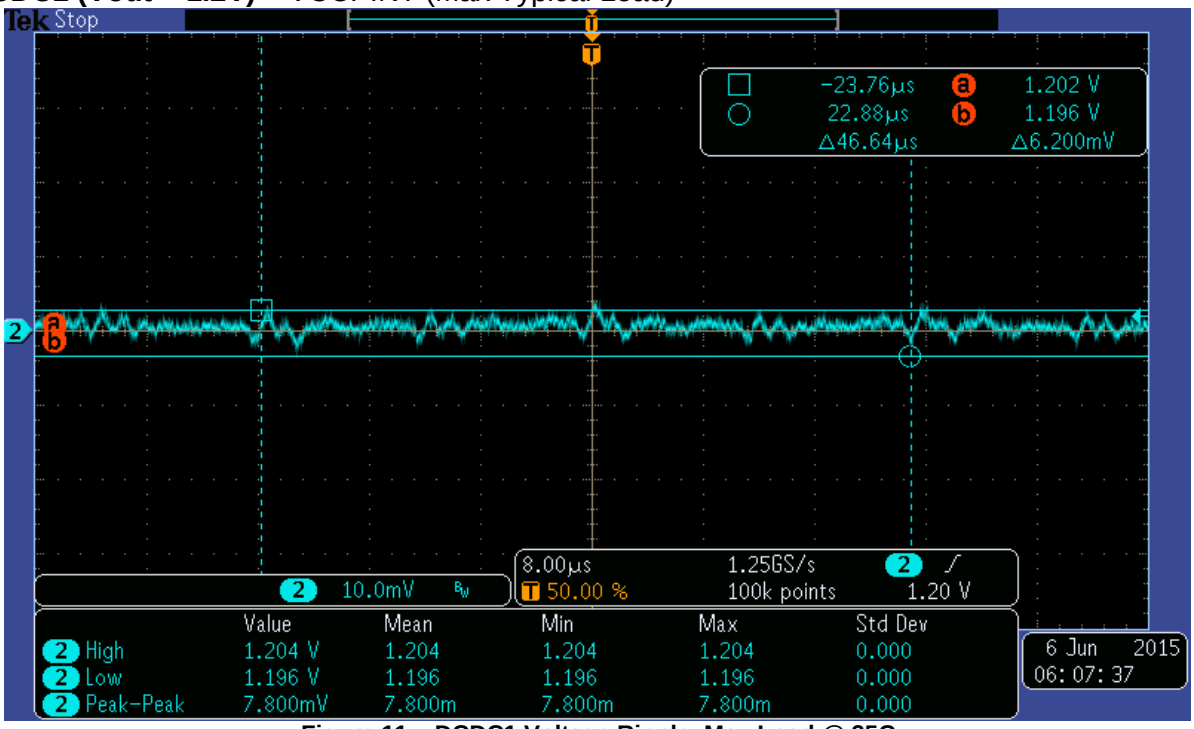


Figure 11 – DCDC1 Voltage Ripple, Max Load @ 25C

DCDC2 (Vout = 1.2V) – VCCD_PLL (Light Load, PFM Mode)

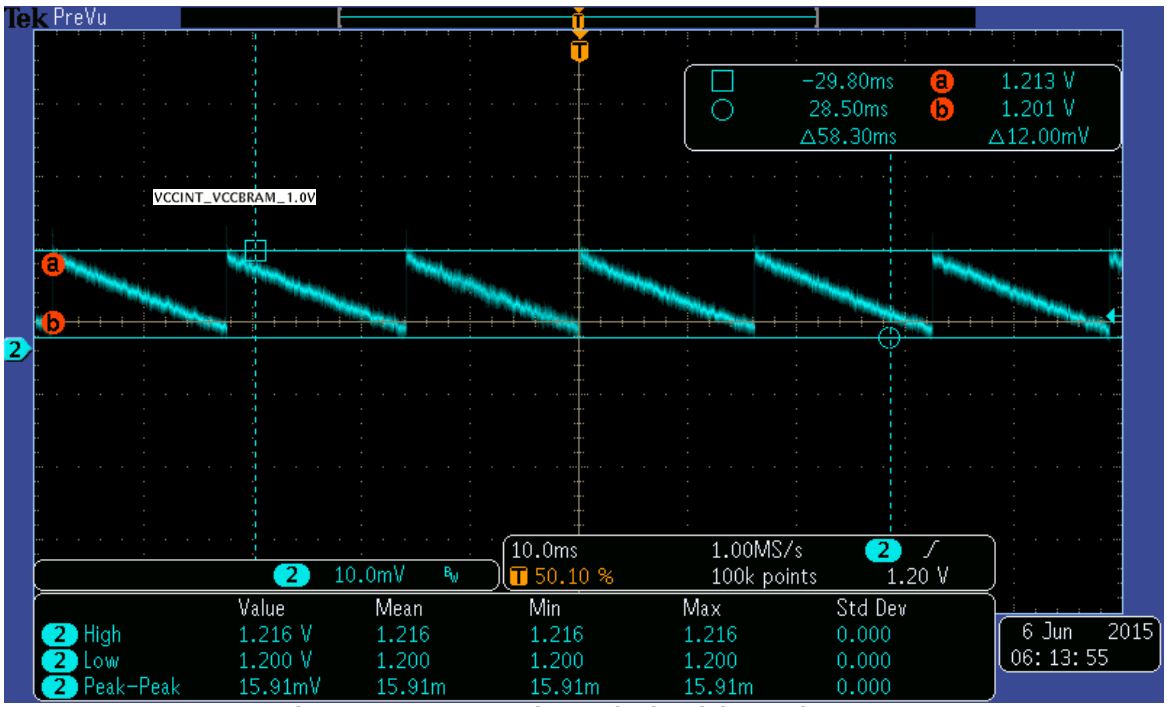


Figure 12 – DCDC2 Voltage Ripple, Light Load @ 25C

DCDC2 (Vout = 1.2V) – VCCD_PLL (Max Typical Load)

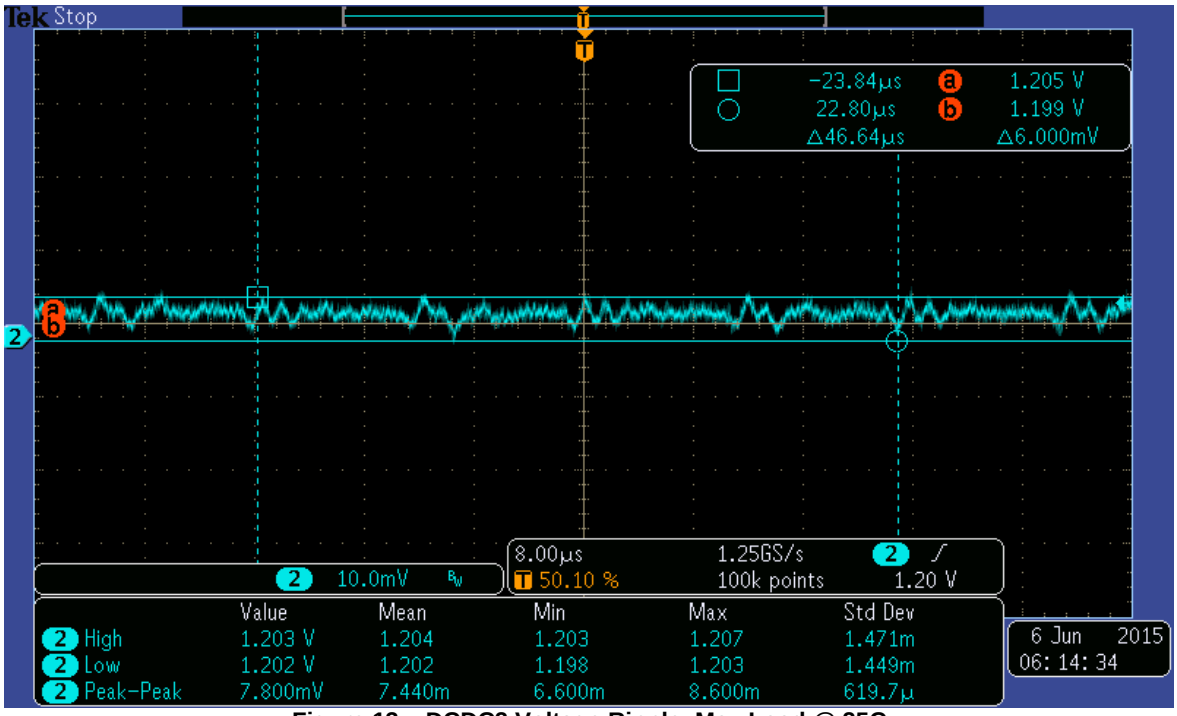


Figure 13 – DCDC2 Voltage Ripple, Max Load @ 25C

DCDC3 (Vout = 2.5V) – VCCA (Light Load, PFM Mode)

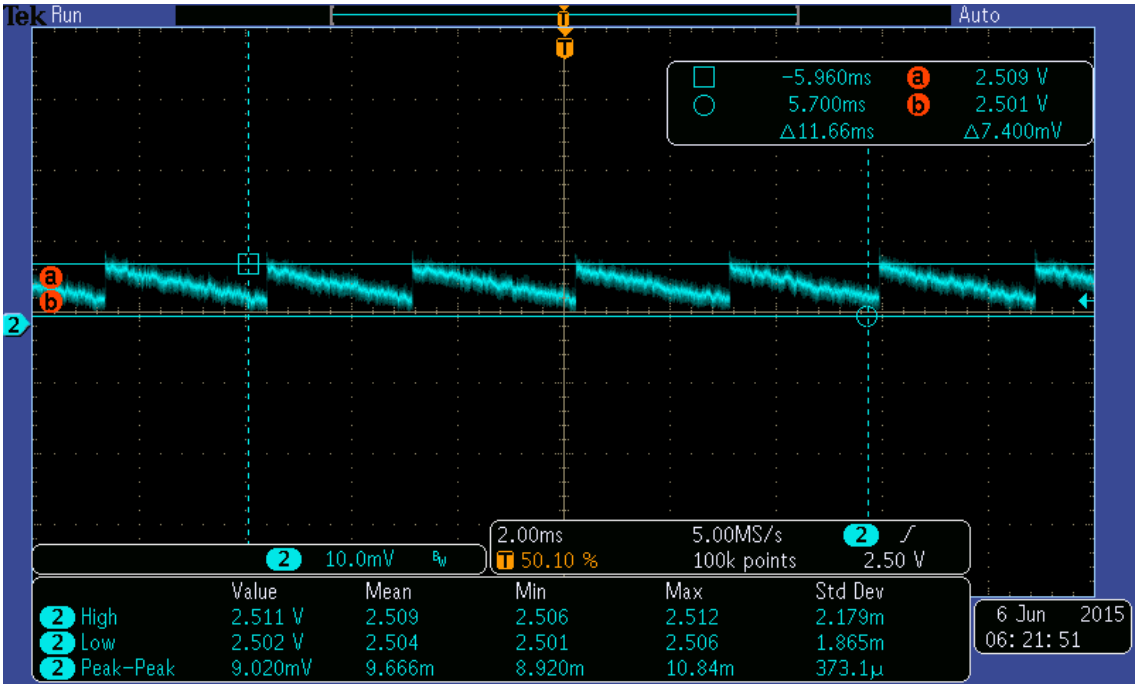


Figure 14 – DCDC3 Voltage Ripple, Light Load @ 25C

DCDC3 (Vout = 2.5V) – VCCA (Max Typical Load)

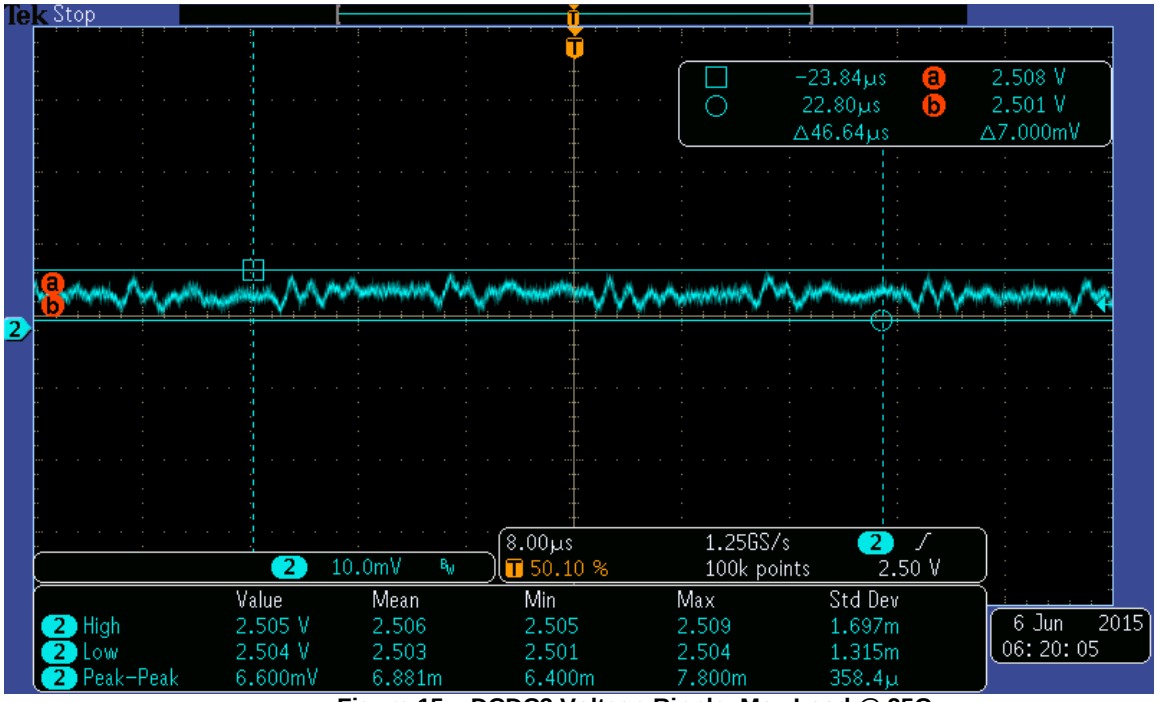


Figure 15 – DCDC3 Voltage Ripple, Max Load @ 25C

Load Transients (Return to Top)

Load transients for each of the DC-DC converters were completed by applying a load step of 0mA to around 50% of the max load for the converter under test. Rise time and fall time were both set at 15µS. The regulators surpass specifications set for the Altera Cyclone Family.

DCDC1 (Vout = 1.2V) – VCCINT Load Step (0mA to 700mA, Rise Time: 15µS; Fall Time:15µS)

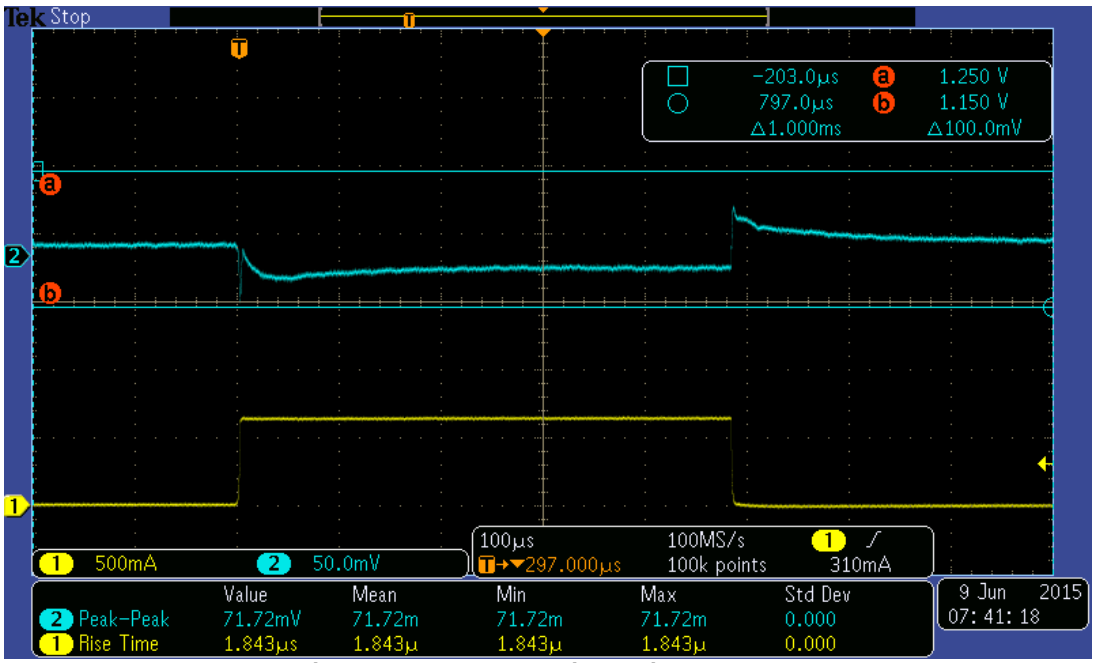


Figure 16 – DCDC1 Load Transient Response @ 25C

DCDC2 (Vout = 1.2V) – VCCD_PLL Load Step (0mA to 500mA, Rise Time: 15µS; Fall Time:15µS)

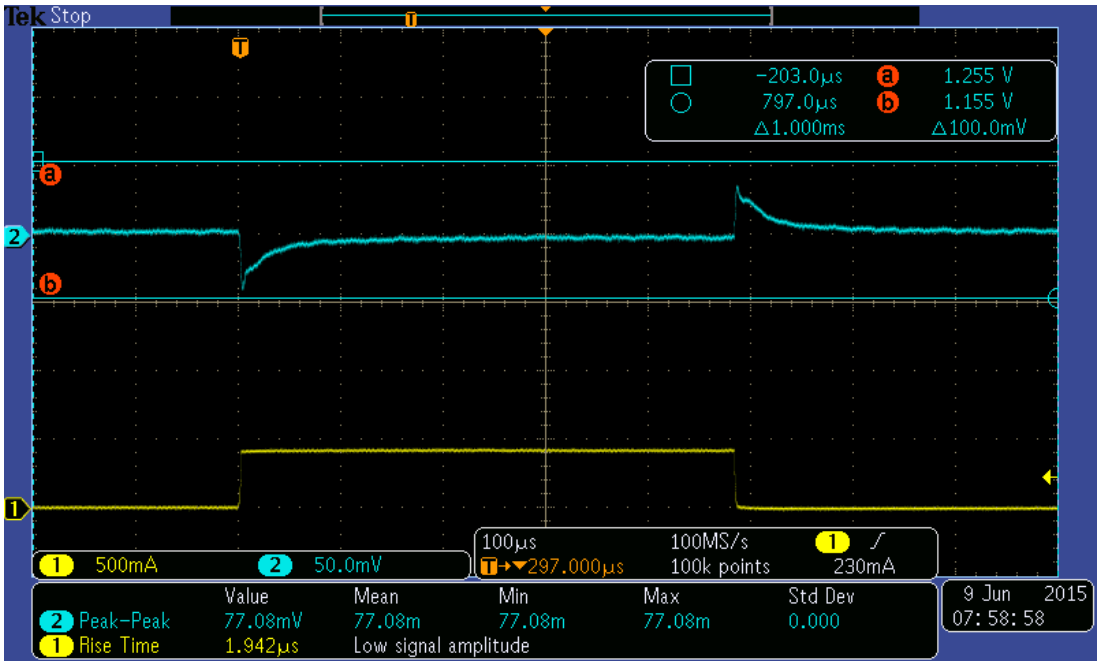


Figure 17 – DCDC2 Load Transient Response @ 25C

DCDC3 (Vout = 2.5V) – VCCO_DDR, VCCO_1.5V Load Step (0mA to 500mA, Rise Time: 15µS; Fall Time:15µS)

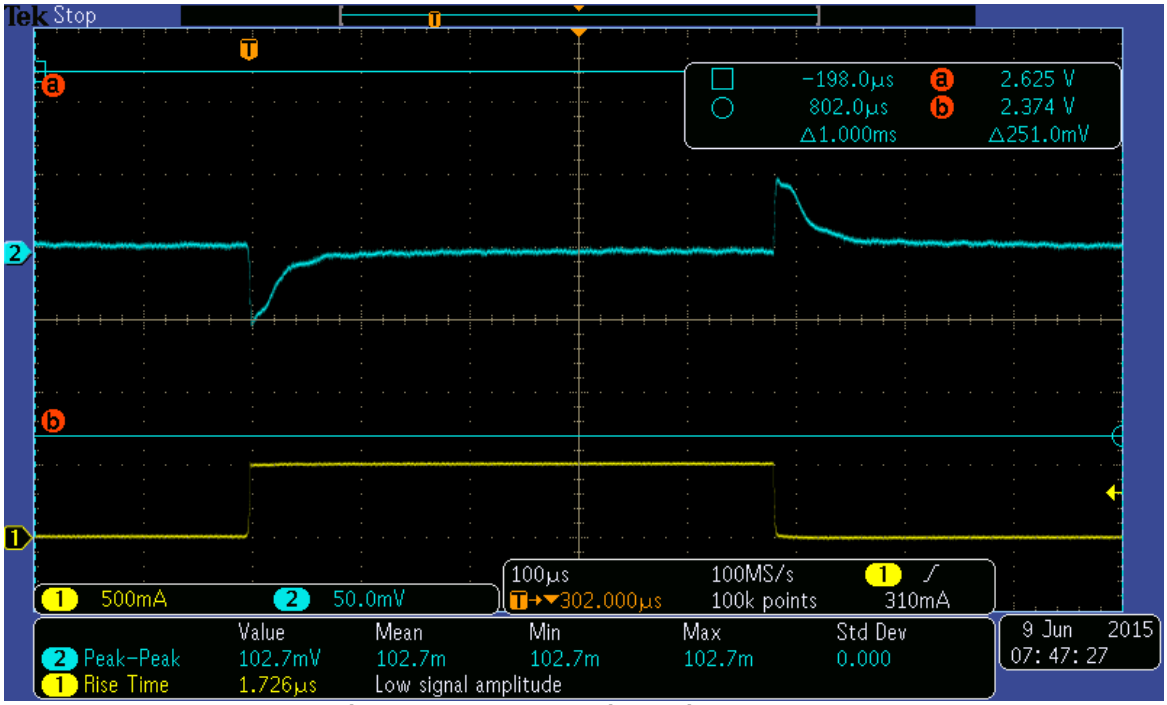


Figure 18 – DCDC3 Load Transient Response @ 25C

Design Considerations (Return to Top)

Altera® Cyclone® III Recommended Power Considerations

For reference, the power requirements from the Altera Cyclone III datasheet are shown below:

Power Supply	Description
V_{CCINT}	Core voltage power supply
V_{CCIO}	I/O power supply to the input and output buffers in Bank 1 to Bank 6
V_{CCA}	Analog power supply for PLL
V_{CCD_PLL}	Digital power supply for PLL
V_{REF} (See Below)	Input reference voltage for voltage-references I/O standards

VCCIO and VREF Design Considerations

The VCCIO pin connections depend on the design's I/O standards, and support 1.2, 1.5, 1.8, 2.5, 3.0 and 3.3 V. Each bank can support a different voltage level. The VREF pin serves as an input reference voltage for the voltage reference I/O standards and is used mainly for a voltage bias and does not source or sink much current. The voltage can be created with a regulator or a resistor divider network. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins

Cyclone III Noise Reduction

To reduce system noise, it is important to ensure that the power supply is clean. Place a ferrite bead and bulk parallel capacitors where the power supply enters the board's power plane to filter out the noise to the power plane. Generally, the tantalum capacitors are used for circuits which demand high stability in the capacitance values.

The ferrite bead should be connected in series between the power supply and the power plane, while the capacitors are connected between the power plane and ground, in parallel with each other. Decoupling depends on the design decoupling requirements of the specific board.

TPS65023 Power Sequencing

Though the Altera Cyclone III does not require a specific power sequencing to ensure proper power up and power down, the TPS65023 offers flexible, customer driven power sequencing. This is achieved by providing separate enable pins for each switch-mode converter and a common enable signal for the LDOs. The table below shows the Pins used in the TPS65023 to create a customized, customer driven power sequence.

PIN NAME	I/O	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.8 V, DEFDCDC3 = VCC defaults VDCDC3 to 3.3 V.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 3.3 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 1.2 V, DEFDCDC1 = VCC defaults VDCDC1 to 1.6 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
$\overline{\text{HOT\_RESET}}$	I	The $\overline{\text{HOT\_RESET}}$ pin generates a reset ($\overline{\text{RESPWRON}}$) for the processor.$\overline{\text{HOT\_RESET}}$ does not alter any TPS65023, TPS65023B settings except the output voltage of VDCDC1. Activating $\overline{\text{HOT\_RESET}}$ sets the voltage of VDCDC1 to its default value defined with the DEFDCDC1 pin. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65023, TPS65023B.
$\overline{\text{RESPWRON}}$	O	$\overline{\text{RESPWRON}}$ is held low when power is initially applied to the TPS65023, TPS65023B. The VRTC voltage is monitored: $\overline{\text{RESWPRON}}$ is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. $\overline{\text{RESPWRON}}$ can also be forced low by activation of the $\overline{\text{HOT\_RESET}}$ pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the $\overline{\text{RESPWRON}}$ pin (1 nF typically gives 100 ms).

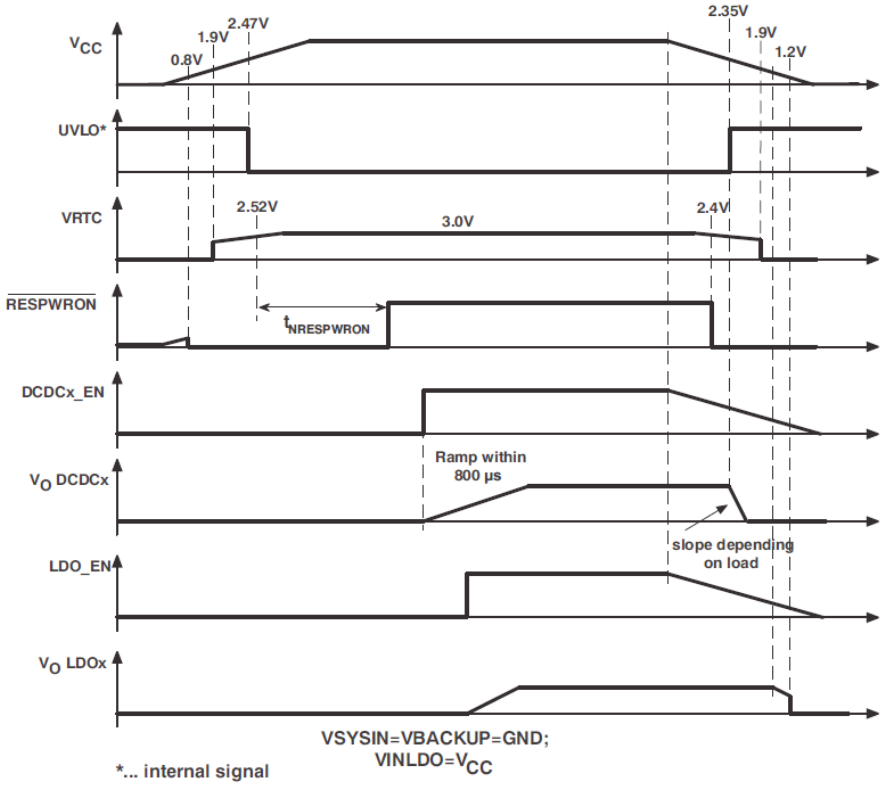


Figure 10 – TPS65023 Example Startup Sequence

Inductor Selection for Buck Converters:

Each of the converters in the TPS65023 typically use a 2.2 µH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. For a fast transient response, a 2.2-µH inductor in combination with a 22-µF output capacitor is recommended. The equation below calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with the equation below. This is needed because during heavy load transient the inductor current rises above the value calculated.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

with:

f = Switching Frequency (2.25 MHz typical)

L = Inductor Value

ΔI_L = Peak-to-Peak inductor ripple current

I_{LMAX} = Maximum Inductor current

The following inductors have been used with the TPS6023:

Device	VALUE	TYPE	MANUFACTURER
All Converters	2.2 µH, 2.5 A, 100 mΩ	LPS4012-222LMB	Coilcraft
	2.2 µH, 1.7 A, 59 mΩ	VLCF4020T-2R2N1R7	TDK
For DCDC2 or DCDC3	2.2 µH, 1.6 A, 90 mΩ	LQH32PN2R2NN0	Murata
For DCDC1	1.5 µH, 1.75 A, 68 mΩ	LQH32PN1R5NN0	Murata
All Converters	2.2 µH, 2.2 A, 80 mΩ	PST25201B-2R2MS	Cyntec

Output Capacitor Selection

TPS65023, TPS65023B allow the use of small ceramic capacitors with a typical value of 10 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended.

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22µF	1206	TDK C3216X5R0J226M	Ceramic
22µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22µF	0805	TDK C2012X5R0J226MT	Ceramic
22µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10µF	0805	TDK C2012X5R0J106M	Ceramic

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each dc-dc converter requires a 10-µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the dc-dc converters. A

filter resistor of up to 10R and a 1-µF capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the VCC pin when all converters are running in PWM mode.

Low Ripple Mode

Low ripple mode can be enabled over I2C for all the DCDC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.5V and 6.0V. This input supply can be from a single cell Li-Ion battery or other externally regulated supply. The low power section of the control circuit for the step-down converters DCDC1, DCDC2 and DCDC3 is supplied by the Vcc pin while the circuitry with high power such as the power stage is powered from the VINDCDC1, VINDCDC2 and VINDCDC3 pins. For proper operation of the step-down converters, VINDCDC1, VINDCDC2,VNDCDC3 and Vcc need to be tied to the same voltage rail. Step-down converters that are planned to be not used, still need to be powered from their input pin on the same rails than the other step-down converters and Vcc.

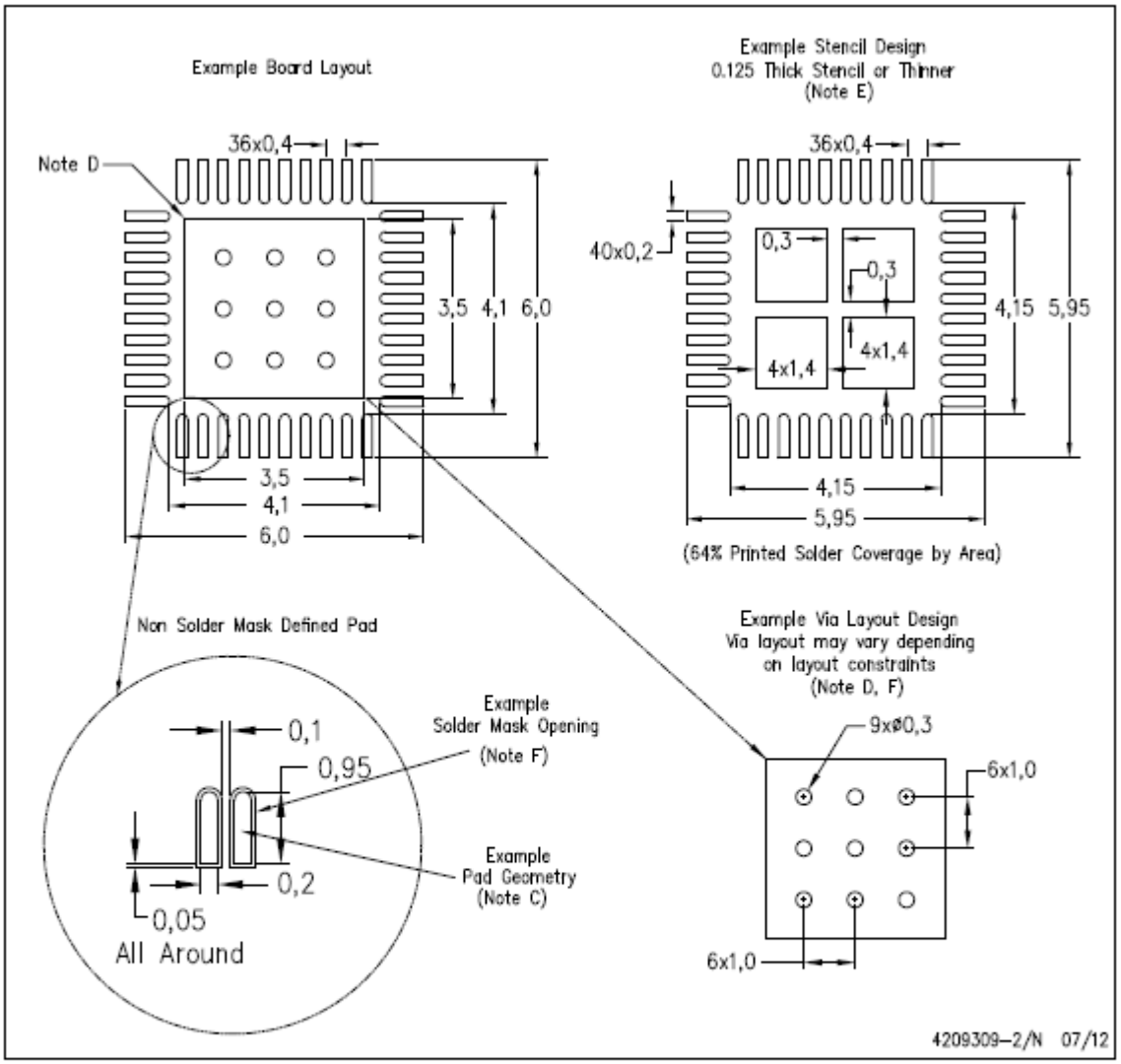
LDO1 and LDO2 share a supply voltage pin which can be powered from the Vcc rails or from a voltage lower than Vcc e.g. the output of one of the step-down converters as long as it is operated within the input voltage range of the LDOs. If both LDOs are not used, the VINLDO pin can be tied to GND.

Layout Guidelines

- Provide a low impedance ground path
  - Use wide and short traces for the main current paths.
- The input capacitors should be placed as close as possible to the IC pins as well as the inductor and output capacitor
- Connect the PGND pins of the device to the PowerPAD™ land of the PCB
- Connect the analog ground connections (AGND) to the PGND at the PowerPAD™
- Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise.
- The VDCDCx line should be connected right to the output capacitor and routed away from noisy components and traces

QFN Package Information

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265