TIDA-00621 Test Report
Powering the i.MX6 Dual/Quad with TPS65911 Power Management IC

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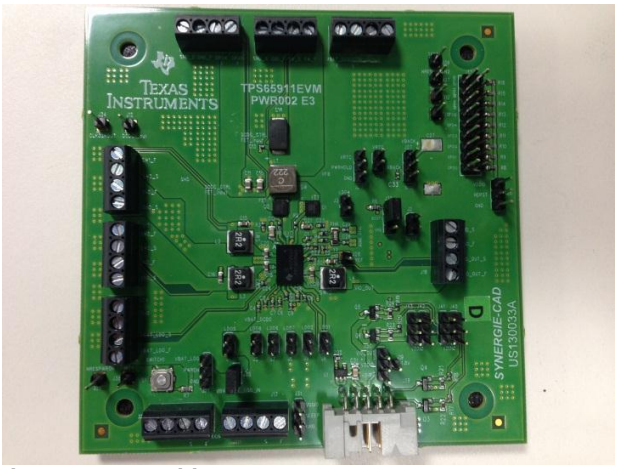


Figure 1 - Top Side

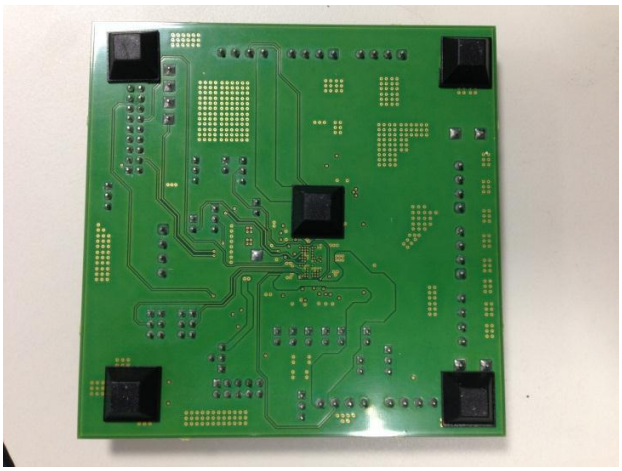


Figure 2 - Bottom Side

Report Contents

Feature Applications

- Factory Automation
- Motor Control
- Smart Grid
- Solar Inverters

Description

TIDA-00621 utilizes a power management integrated circuit (PMIC) for supplying a Freescale® i.MX6 SoC in a DDR3 application. This design showcases the TPS65911 as an all-in-one IC used to supply the rails needed for powering the i.MX6 SoC, with available regulators for system peripherals. The TPS65911 offers simple, flexibile output voltages and sequencing. The voltages on the DC/DC converters can be adjusted over i2c once the device has entered the active state, allowing for individual regulator customization.

TPS65911/i.MX6 Block Diagram (Return to Top)

Power Supply Block Diagram

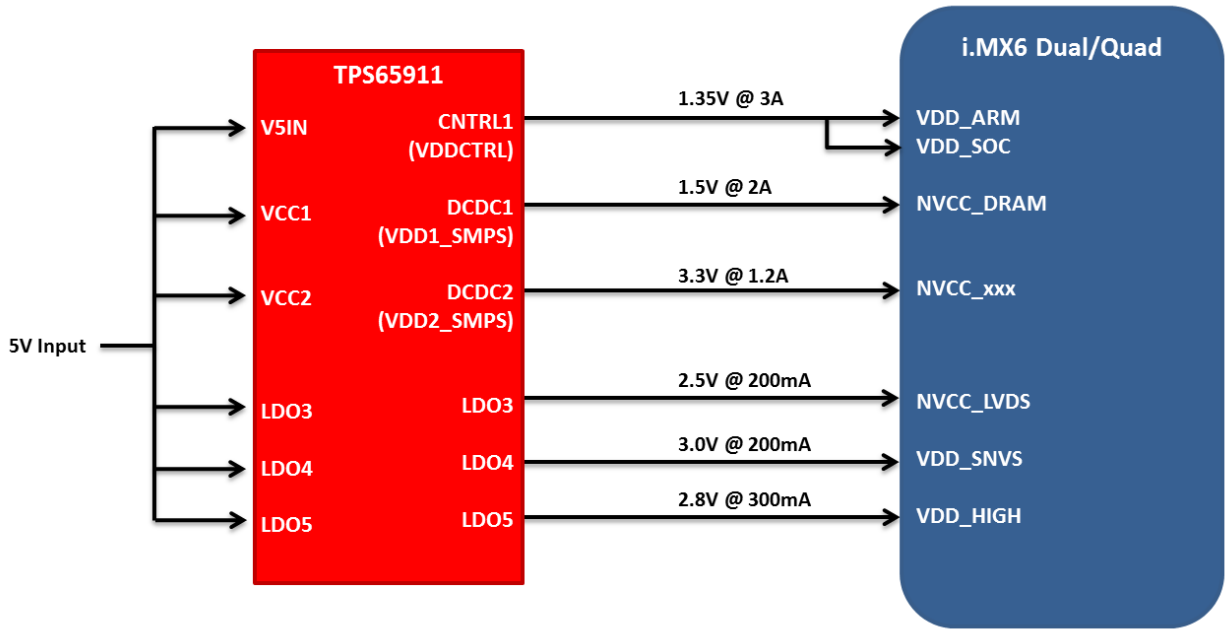


Figure 3 – IMX6 Block Diagram

Typical Voltage and Current Requirements in End Applications

Depending on the application, current consumption of the i.MX6 power rails can vary. The table below highlights the typical max currents each power output of the TPS65911 PMIC may supply to the IMX6 rails.

IMX6 Supply Rails	Voltage	Current Consumption (mA)
VDD_SNVS	3.0V	200
VDD_ARM	1.35V	Component Specific
VDD_SOC		
NVCC_xxx	3.3V	1200
NVCC_LVDS	2.5V	200
VDD_HIGH	2.8V	300
NVCC_DRAM (DDR3)	1.5V	2000

Note: *NVCC_LVDS powers the pre-drivers for the DDR I/O pins, and must be powered even when LVDS is not used. The maximum current consumption of a design will vary depending on the specific application.*

Efficiency Curves (Return to Top)

VDD1 (Vin=5V, Vout=1.5V, PWM) – *NVCC_DRAM*

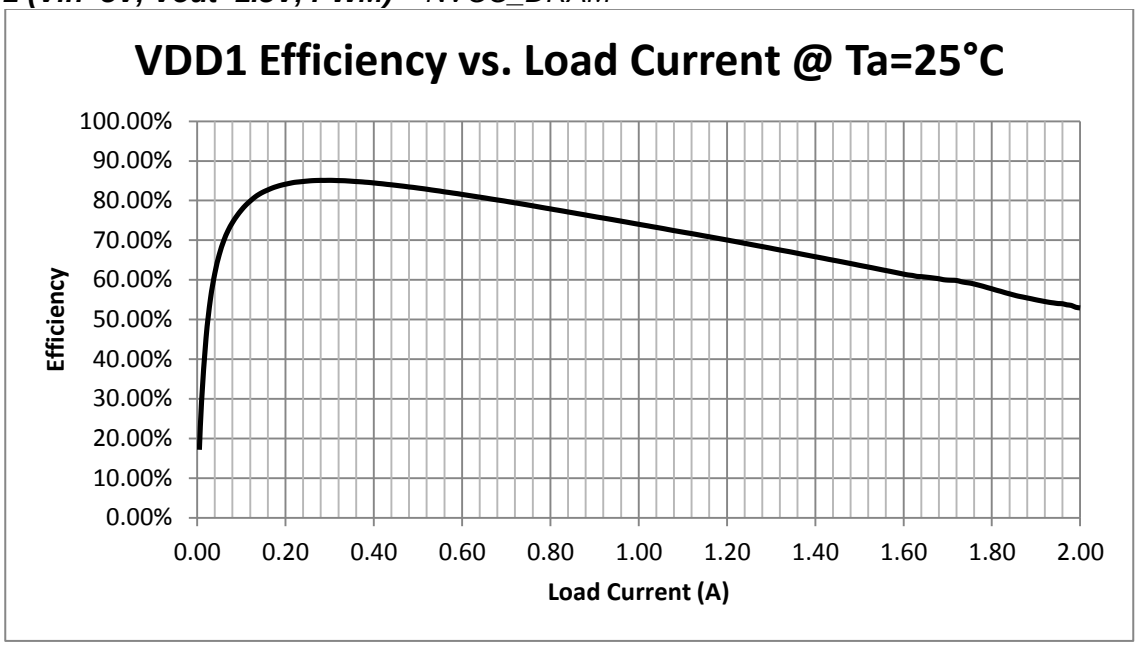


Figure 4 - DCDC1 Efficiency @ 25C

VDD2 (Vin=5V, Vout=3.3V, PWM) – *NVCC_xxx*

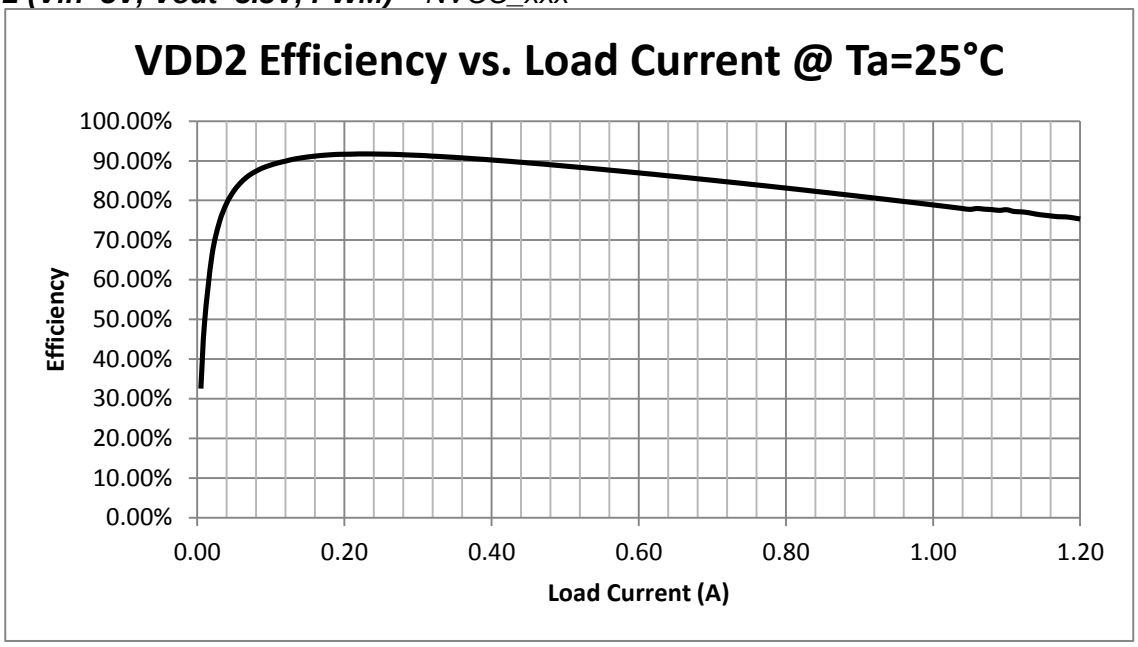


Figure 5 – DCDC2 Efficiency @ 25C

VIO (Vin=5V, Vout=1.5V, PWM) – *Peripherals*

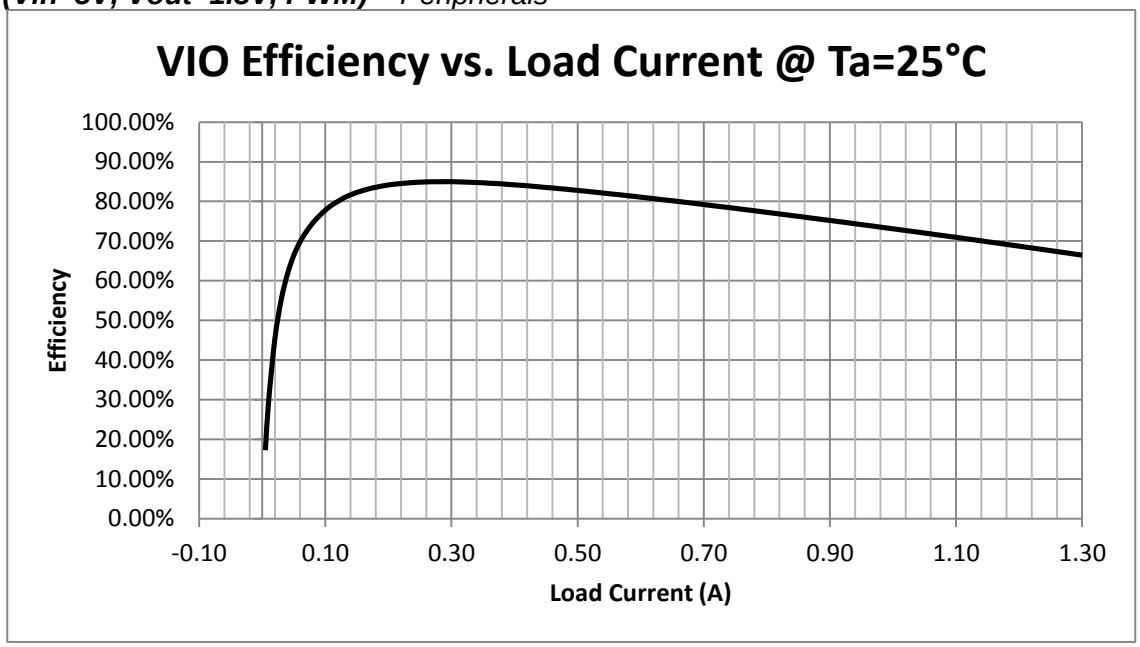


Figure 6 – VIO Efficiency @ 25C

VDDCTRL (Vin=5V, Vout=1.35V, PWM) – *VDD_ARM_IN, VDD_SOC_IN*

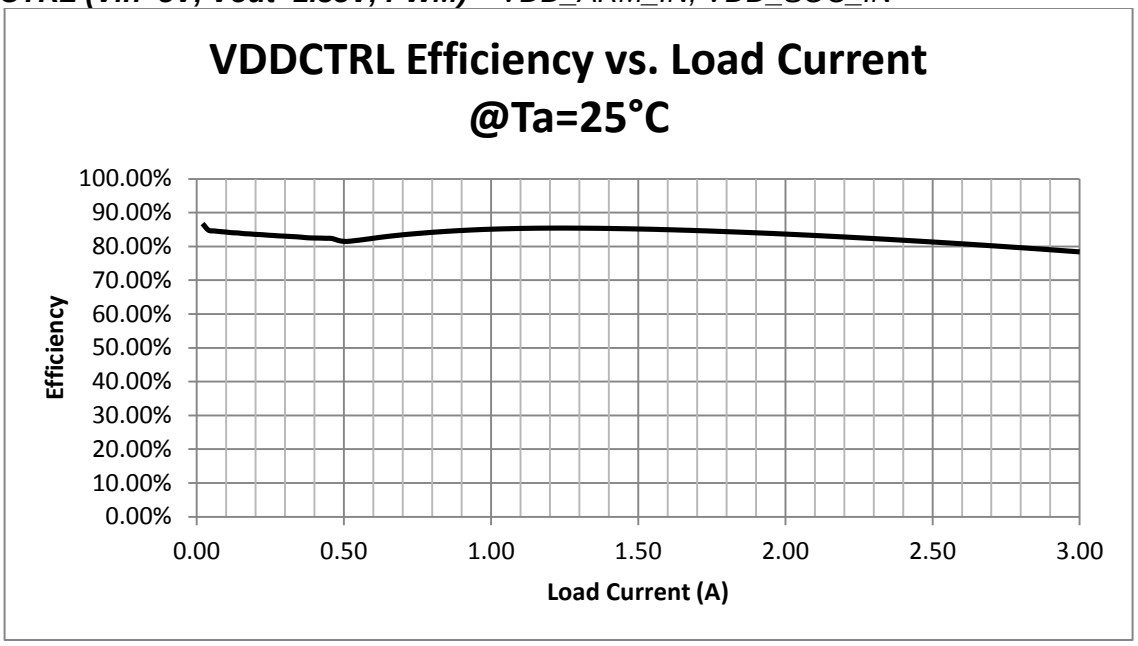


Figure 7 – CTRL1 Efficiency @ 25C

Load Regulation (Return to Top)

VDD1 (Vin=5V, Vout=1.5V, PWM) – *NVCC_DRAM*

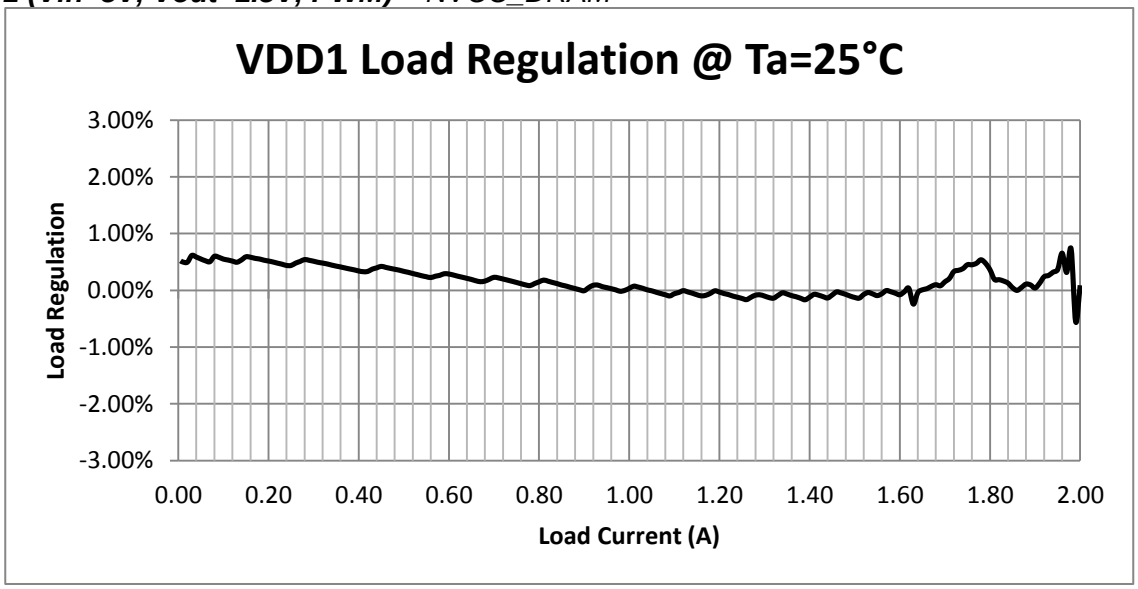


Figure 8 – DCDC1 Load Regulation @ 25C

VDD2 (Vin=5V, Vout=3.3V, PWM) – *NVCC_xxx*

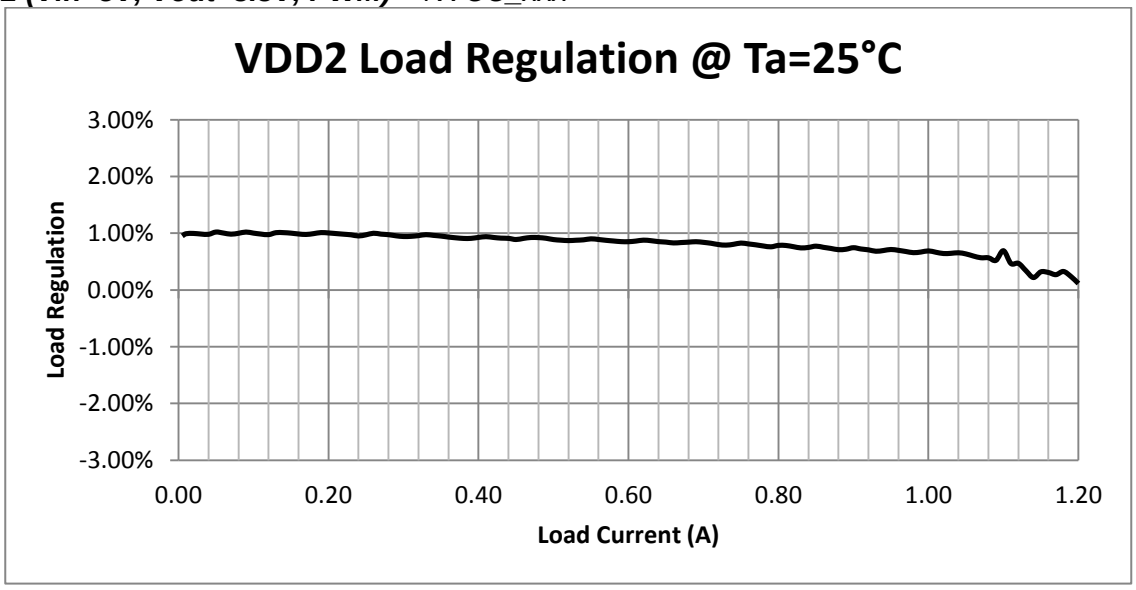


Figure 9 – DCDC2 Load Regulation @ 25C

VIO (Vin=5V, Vout=1.5V, PWM) – *Peripherals*

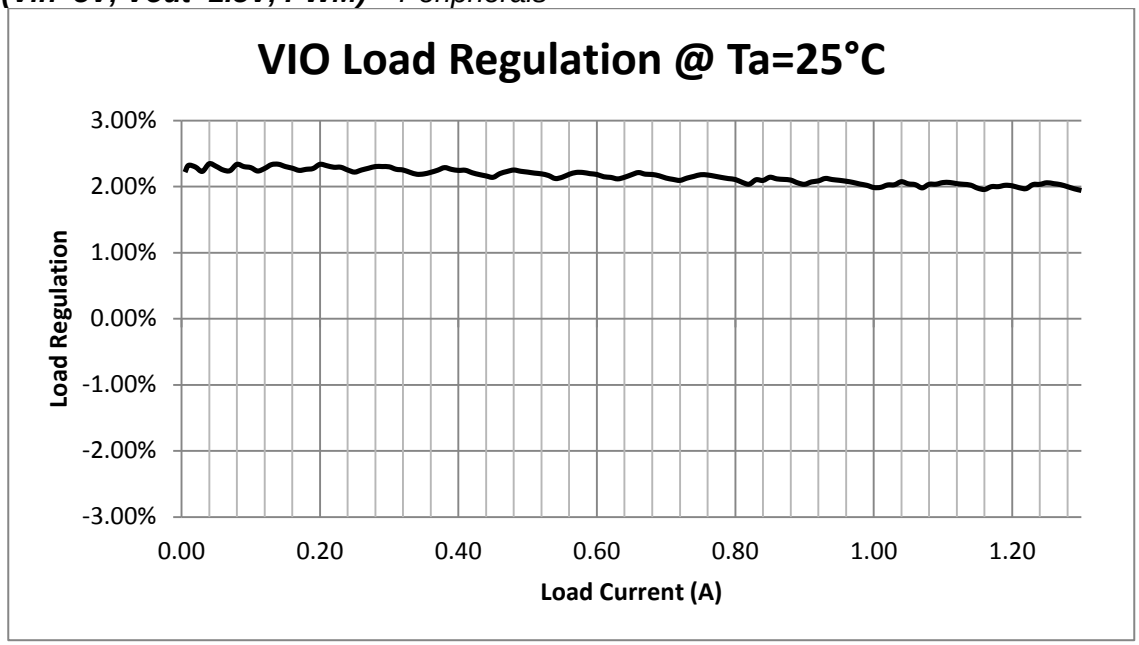


Figure 10 – VIO Load Regulation @ 25C

VDDCTRL (Vin=5V, Vout=1.35V, PWM) – *VDD_ARM_IN, VDD_SOC_IN*

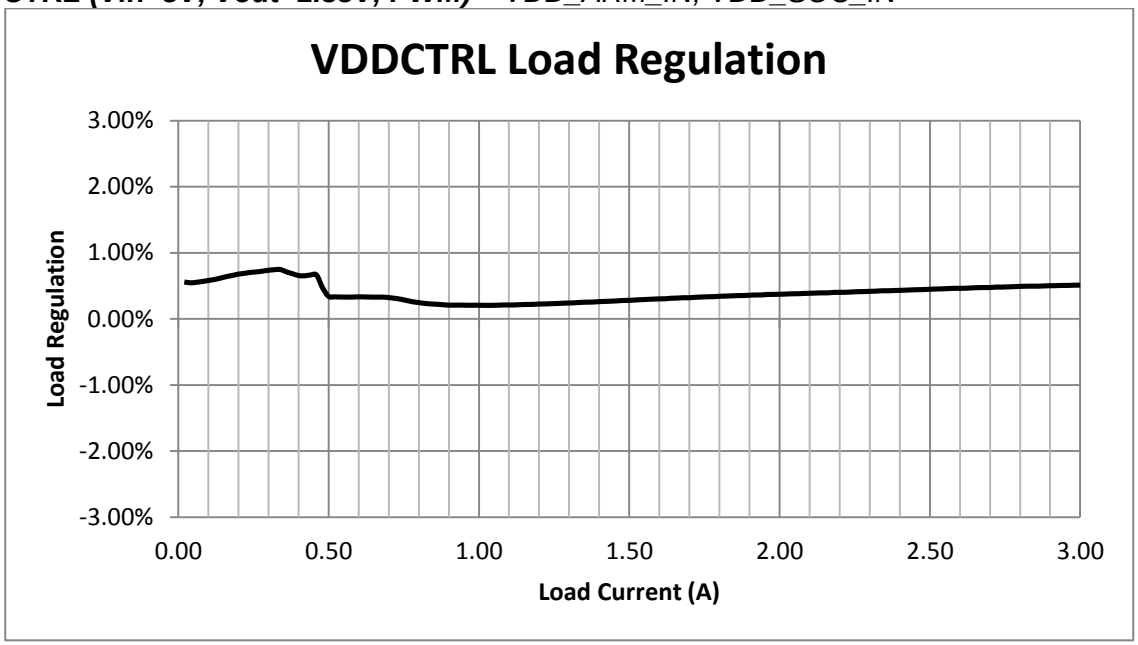


Figure 11 – *CTRL1* Load Regulation @ 25C

Output Ripple Voltage (Return to Top)

VDD1 (Vin=5V, Vout=1.5V, PWM) – *NVCC_DRAM* (2000mA Load)

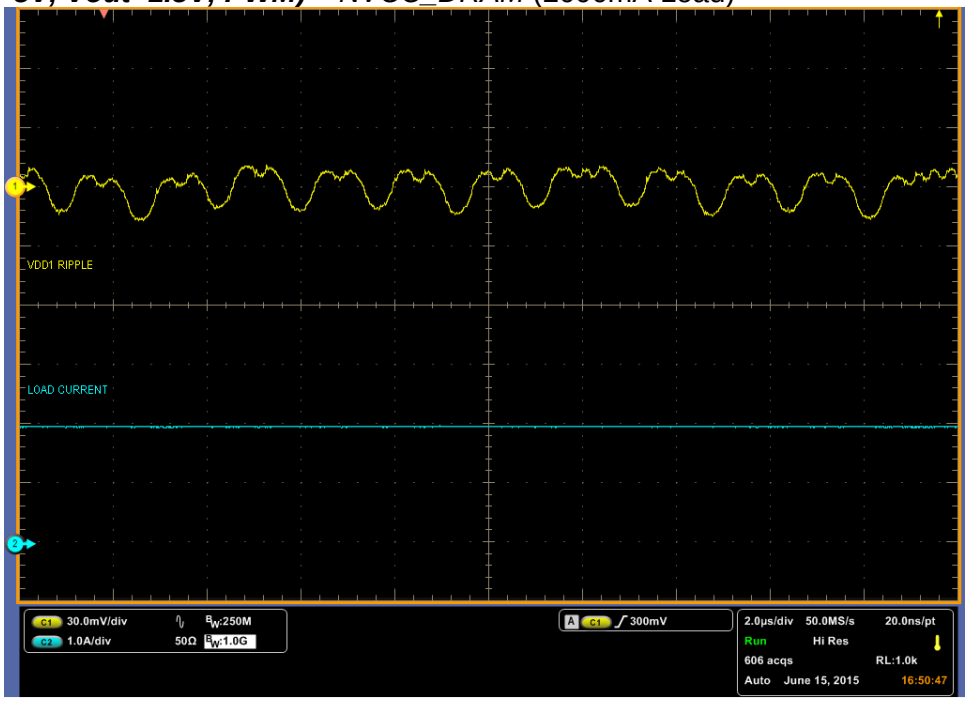


Figure 12 – *DCDC1* Voltage Ripple @ 25C

VDD2 (Vin=5V, Vout=3.3V, PWM) – *NVCC_xxx* (1000mA Load)

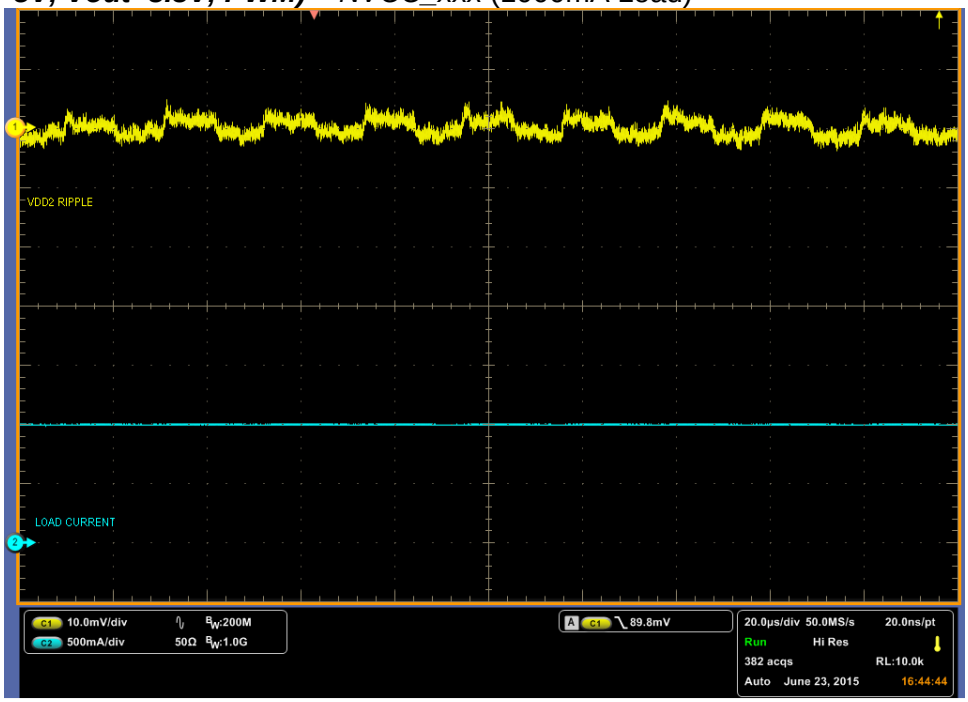


Figure 13 – *DCDC2* Voltage Ripple @ 25C

VIO (Vin=5V, Vout=1.5V, PWM) – *Peripherals* (1300mA Load)

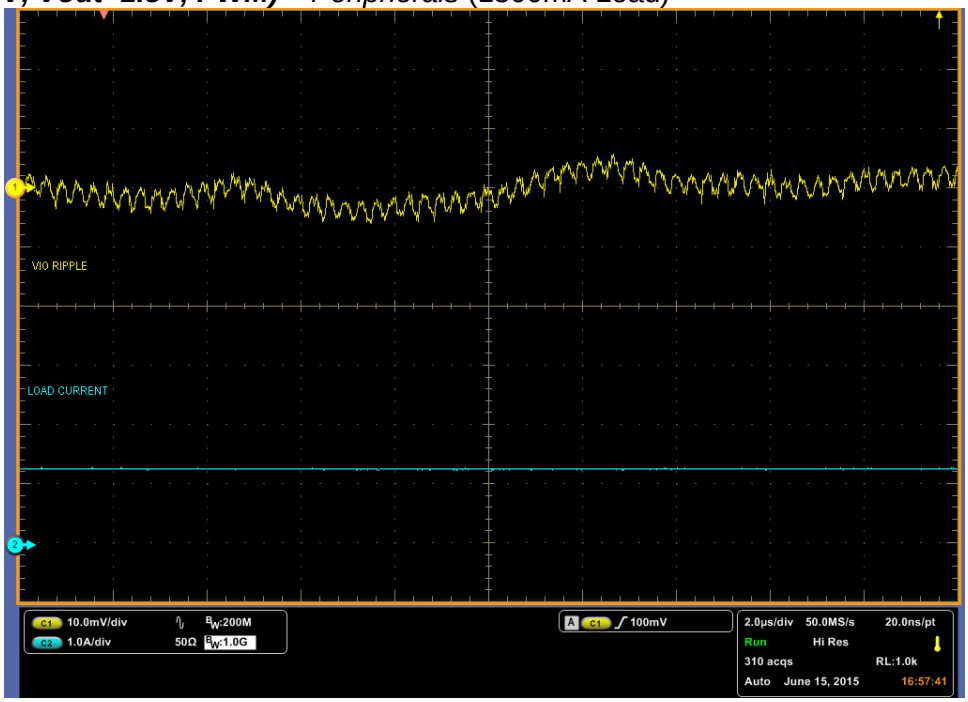


Figure 14 – *VIO* Voltage Ripple @ 25C

VDDCTRL (Vin=5V, Vout = 1.35V, PWM) – *VDD_ARM_IN, VDD_SOC_IN* (3000mA Load)

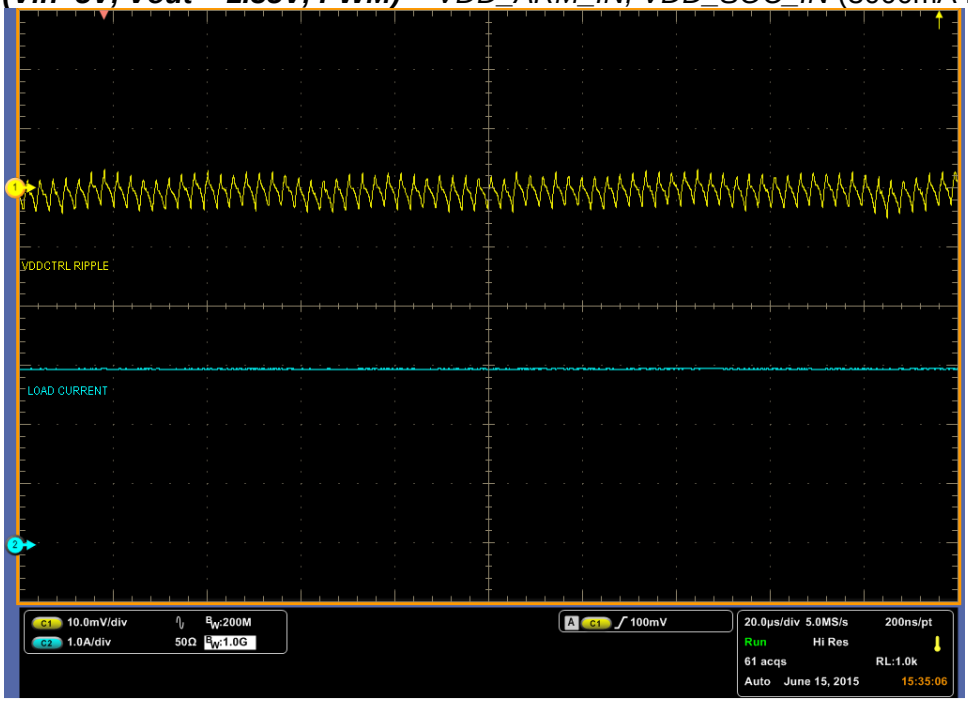


Figure 15 – *VDDCTRL* Voltage Ripple @ 25C

Load Transients (Return to Top)

Load transients for each of the DC-DC converters were completed by applying a current load step of approximately 25% to 75% of the max load for the regulator under test. Rise time and fall time were both set at ~100mA/µS for the converters (VDD1, VDD2), and ~200mA/µS for the controller (VDDCTRL).

VDD1 (Vin=5V, Vout = 1.5V, PWM) – *NVCC_DRAM (300mA to 800mA, Rise Time: 5µS; Fall Time: 5µS)*

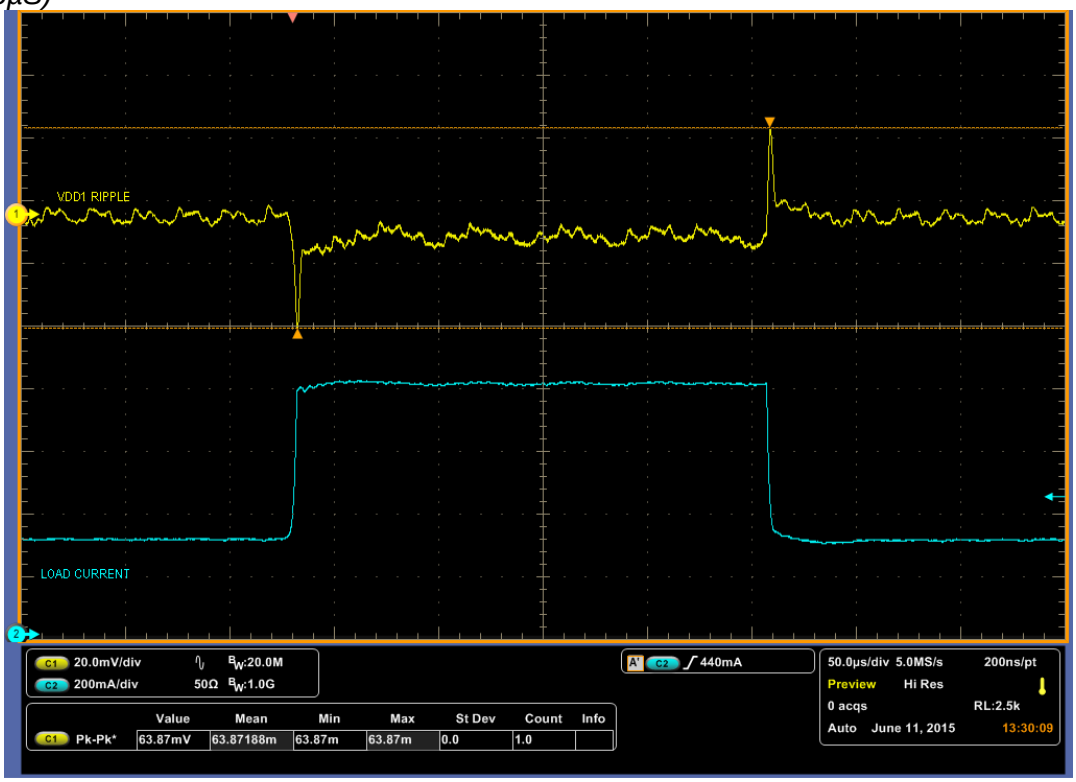


Figure 16 – *DCDC1* Load Transient @ 25C

VDD2 (Vin=5V, Vout = 3.3V, PWM) – *NVCC_xxx (300mA to 800mA, Rise Time: 5µS; Fall Time: 5µS)*

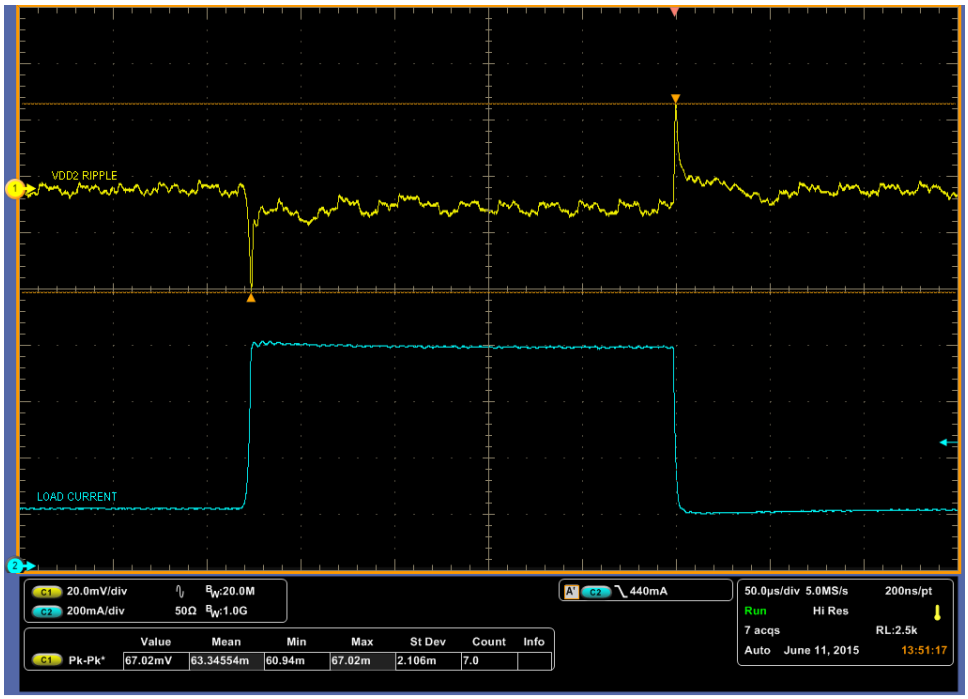


Figure 17 – *DCDC2* Load Transient @ 25C

VIO (Vin=5V, Vout = 1.5V, PWM) – *Peripherals (300mA to 800mA, Rise Time: 5µS; Fall Time: 5µS)*

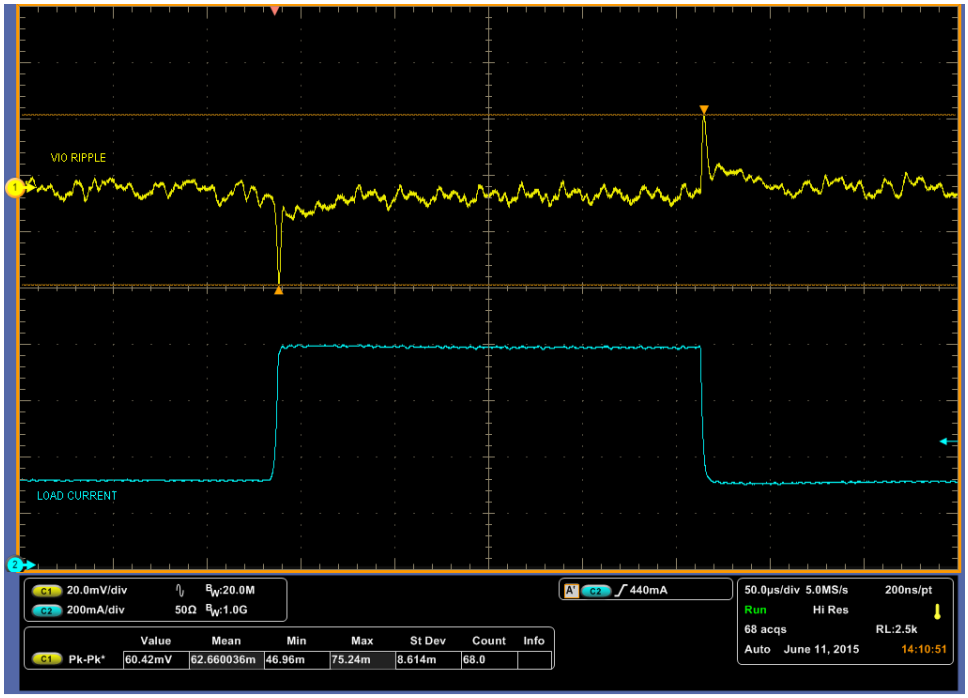


Figure 18 – *VIO* Load Transient @ 25C

VDDCTRL (Vin=5V, Vout = 1.35V, PWM) – *VDD_ARM_IN, VDD_SOC_IN (800mA to 2000mA, Rise Time: 5µS; Fall Time: 5µS)*

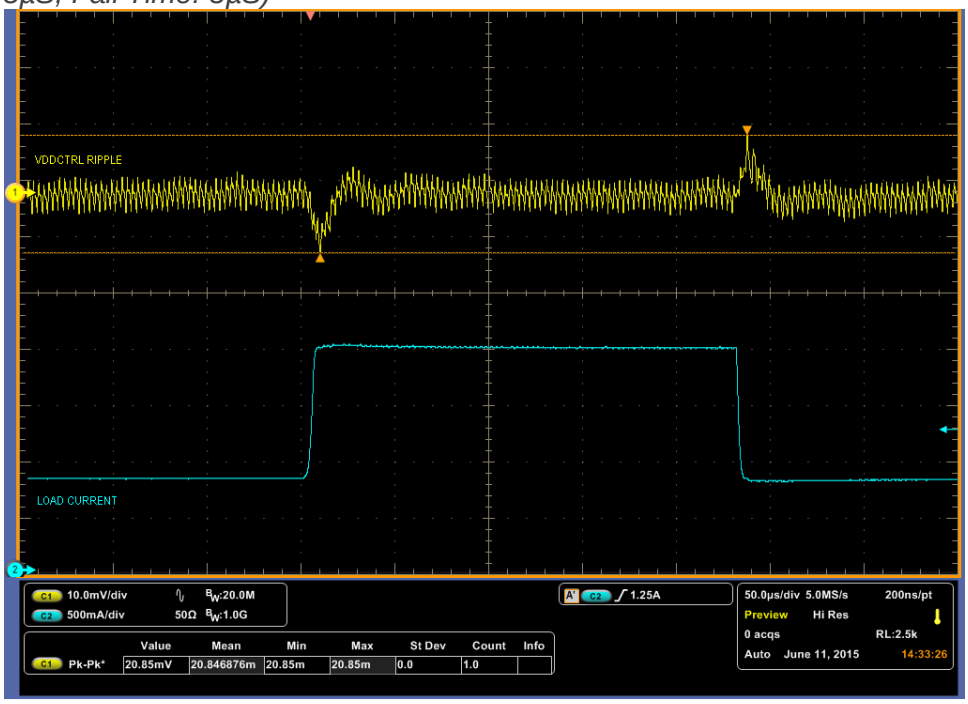


Figure 19 – *VDDCTRL* Load Transient @ 25C

Start-up Sequence (Return to Top)

Regulator sequencing requirements for the i.MX6 are fairly loose, therefore the primary advantage of bringing multiple supplies to their operating voltages at various times manifests in minimizing inrush currents on the input supply rail. By staggering the various voltage rails, lower capacity supplies can better maintain their output voltage during startup. Figure 20 details the complete start-up sequence of the TPS65911 PMIC configured for the IMX6, with load resistors on each rail drawing approximately half of the maximum regulator current.

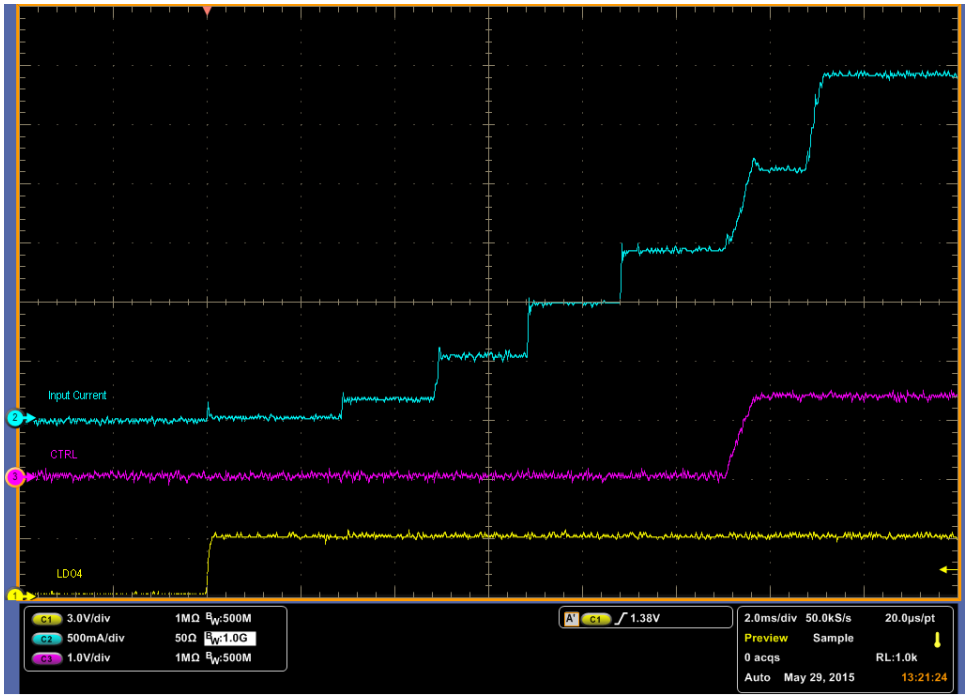


Figure 20 – Power-Up Sequence (Half Max Load) Current Consumption

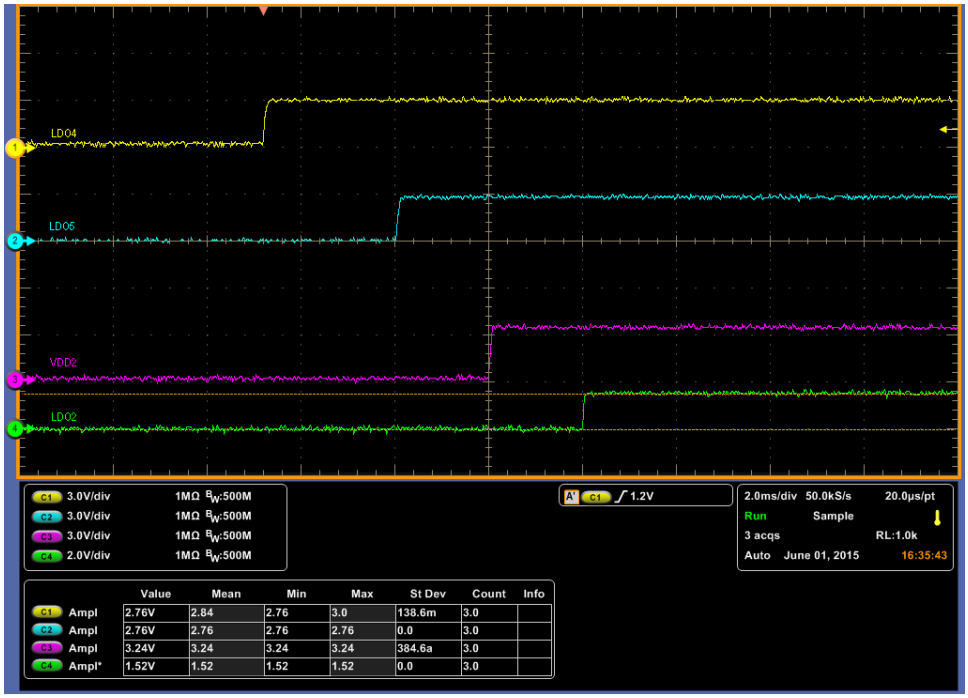


Figure 21 – Power-Up Sequence (No Load) Voltage Waveforms
(LDO4_3.0V, LDO5_2.8V, VDD2_3.3V, LDO2_1.5V)

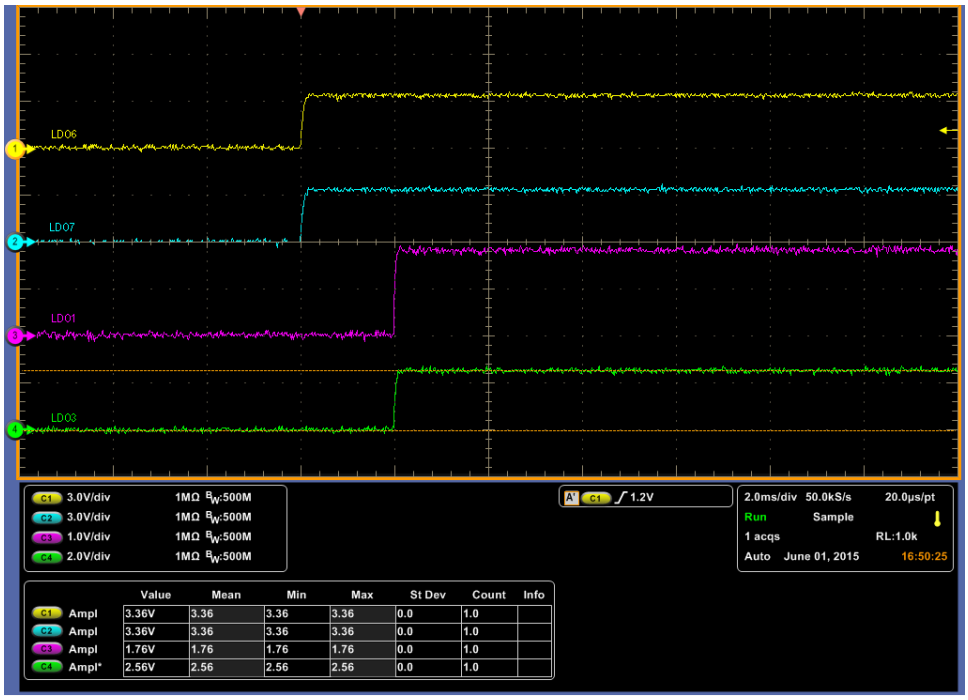


Figure 22 – Power-Up Sequence (No Load) Voltage Waveforms
(LDO6_3.3V, LDO7_3.3V, LDO1_1.8V, LDO3_2.5V)

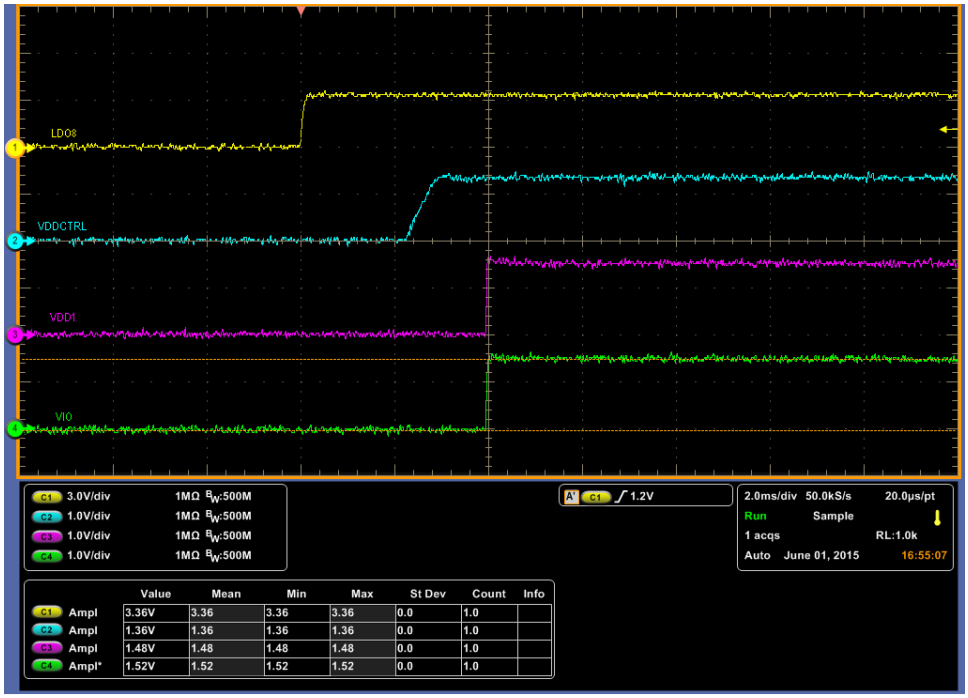


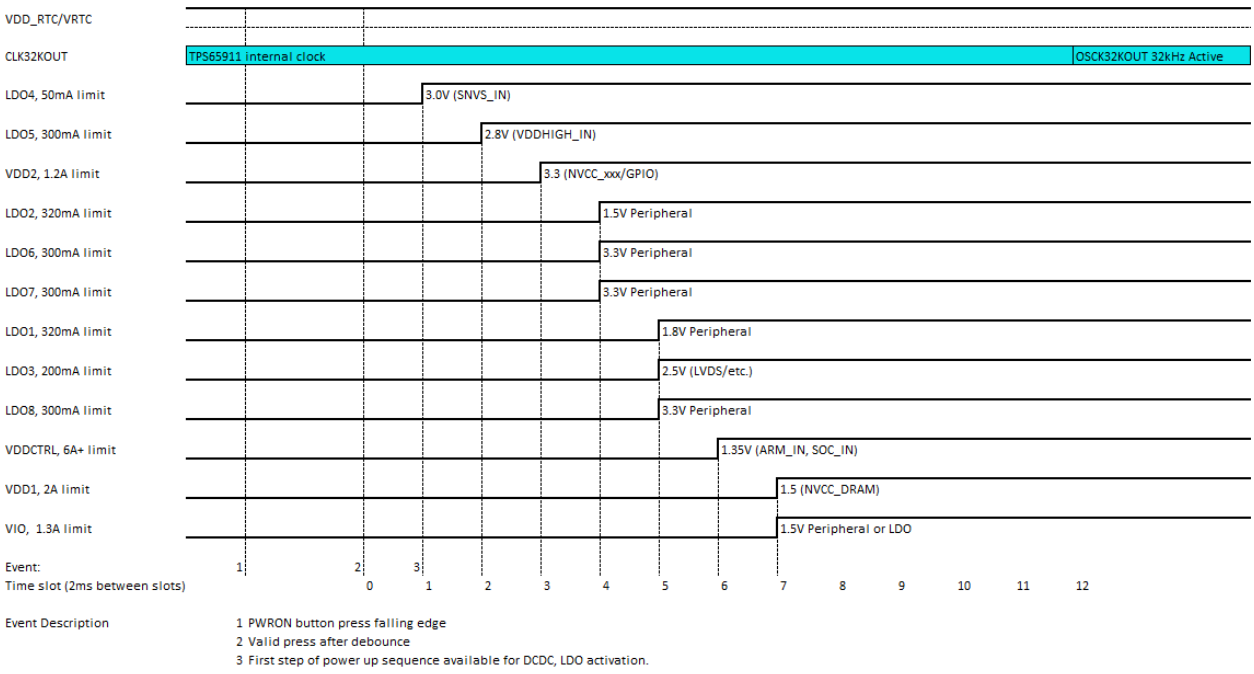
Figure 23 – Power-Up Sequence (No Load) Voltage Waveforms
(LDO8_3.3V, VDDCTRL_1.35V, VDD1_1.5V, VIO_1.5V)

Design Considerations (Return to Top)

Per requirements from Freescale, the supply for VDD_SNVS_IN must be turned on before any other supply. VDD_SNVS_IN can also be shorted to VDD_HIGH_IN, as long as the above requirement is met. There are no special restrictions for powering down the i.MX6 Dual or Quad SoCs.

VDD_ARM_IN and VDD_SOC_IN may be supplied from the same source. If VDD_SOC_IN and VDD_ARM_IN are powered by separate supplies, VDDSOC_IN can be supplied before VDD_ARM_IN with a maximum delay of 1ms.

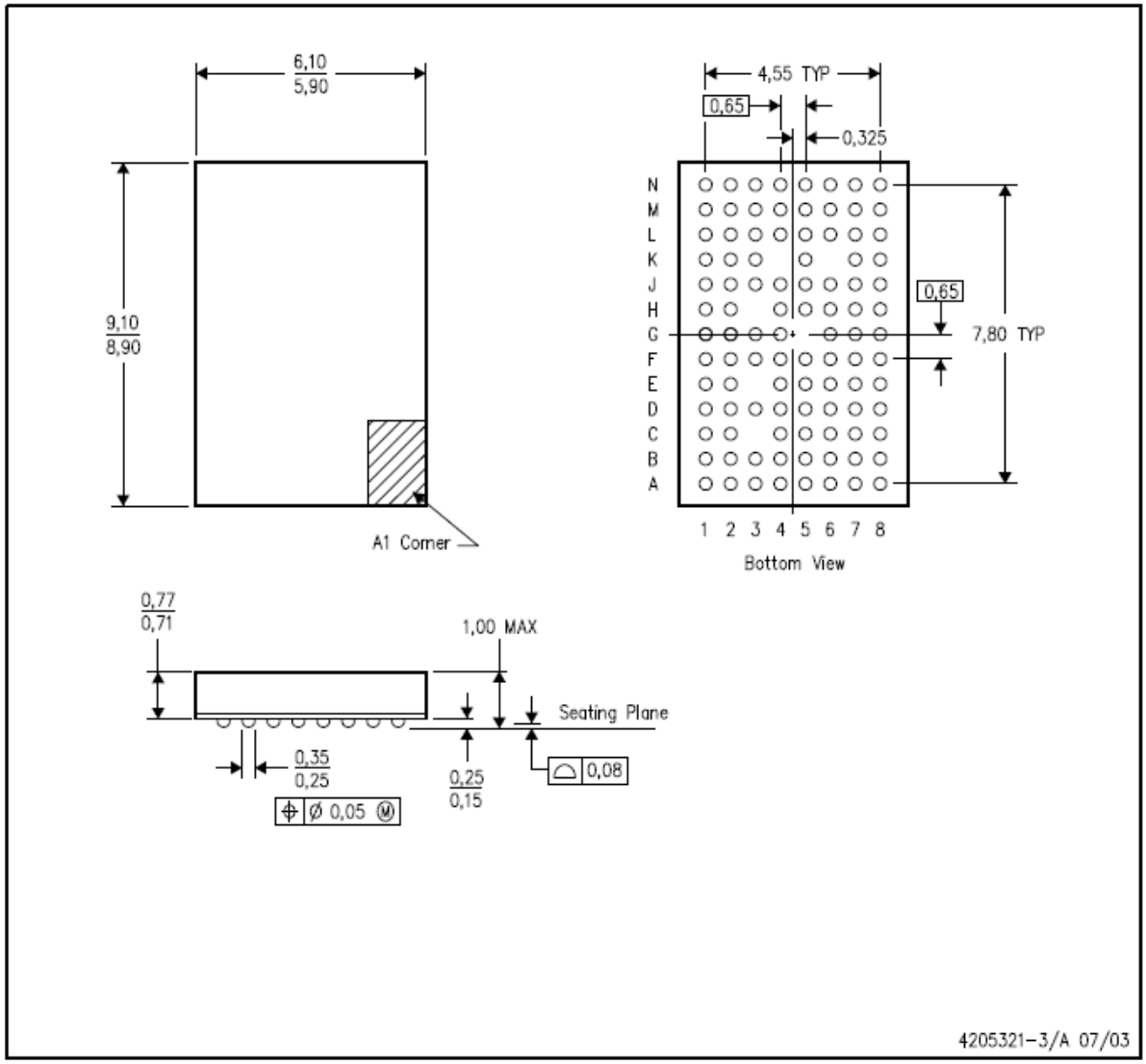
The TPS65911 can be utilized with a coin cell or LDO4 powering SNVS_IN. The following power-up sequence demonstrates compliance of the TPS65911 PMIC with Freescale's recommendations. While the sequencing requirements for the i.MX6 SoC are lax, delaying activation time of each regulator beneficially reduces inrush currents in the overall design and mitigates demand on the system supply.



Additional regulators are intended to supply various peripherals in the full system and may be deactivated after the device has reached an active state. Excluding VRTC, each regulator is adjustable over i2c allowing for custom configurations.

For further design considerations specific to a particular application, please refer to the following Freescale documents: Dual Quad Technical Data (IMX6DQCPOPEC), Dual/Quad Hardware Design Application Note (AN4397), Dual/Quad Power Consumption Application Note (AN4509), TPS659110 Datasheet (SWCS049).

ZRC (S–PBGA–N98) PLASTIC BALL GRID ARRAY



NOTES:
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B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

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